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Thesis submitted to obtain the degree of:

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Control of Open-end Winding Induction Machine Based on Indirect Matrix Converter

Concepción, April 2015

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Nomenclature

Matrices

$\boldsymbol{S_r}$: rectifier switching matrix.

$\boldsymbol{S_{i1}}$: inverter 1 switching matrix.

$\boldsymbol{S_{i2}}$: inverter 2 switching matrix.

Vectors

$\boldsymbol{v_s}$: source voltage vector.

$\boldsymbol{v_i}$: power converter input voltage vector.

$\boldsymbol{v_{o,ph}}$: power converter output phase voltage vector.

$\boldsymbol{i_s}$: source current vector.

$\boldsymbol{i_i}$: power converter input current vector.

$\boldsymbol{i_o}$: power converter output current vector.

$\boldsymbol{i_r}$: machine rotor current vector.

$\boldsymbol{\Psi_s}$: machine stator flux linkage vector.

$\boldsymbol{\psi_2}$: auxiliary vector.

$\boldsymbol{\Psi_r}$: machine rotor flux vector.

Scalars

v_{DC} : DC link voltage.

i_{DC} : DC link current.

m_o : modulation index.

$\hat{V}_{o,ph}$: peak converter output phase voltage.

$\hat{V}_{s,ph}$: peak converter input phase voltage.

$\hat{V}_{s,l-l}$: peak converter input line-to-line voltage.

T : machine torque.

T_L : load torque.

J_m : machine inertia moment.

B_m : machine viscous friction coefficient.

ω_r : machine rotor speed.

v_{cm} : common-mode voltage.

v_{zs} : zero sequence voltage.

Abbreviations

AC	: Alternating Current.
DC	: Direct Current.
DSP	: Digital Signal Processor.
FPGA	: Field Programmable Gate Array.
HPI	: Host Port Interface.
IMC	: Indirect Matrix Converter.
MC	: Matrix Converter.
NPC	: Neutral Point Clamped.
PWM	: Pulse Width Modulation.
SPWM	: Sinusoidal Pulse Width Modulation.
SVM	: Space Vector Modulation.
THD	: Total Harmonic Distortion.
VSI	: Voltage Source Inverter.

Abstract

The aim of this thesis is to study the application of an Indirect Matrix Converter (IMC), with two inverter output stages, to supply energy to an induction machine with opened stator winding (so-called open-end winding connection). This type stator winding connection presents several advantages, compared with a conventional wye or delta connected machines, such as: equal power input from both machine winding ends, thus each inverter is rated at half the machine power rating; each phase stator current can be controlled independently; possibility to have twice the effective switching frequency (depending on the modulation strategy); extensibility to more phases, therefore multiphase induction machines can be considered if current reduction is required; possibility of reducing common-mode voltage; and certain degree of fault tolerance, as there is voltage space vector redundancy.

However, an open-end winding induction machine drive can have some drawbacks, such as: possibility of zero sequence current flow through the machine, this because of the occurrence of zero sequence voltage; increased conduction losses; higher complexity in the power converter requirements, i.e. more power devices, circuit gate drives, etc.

On the other hand, the use of an IMC to drive this machine presents the following features: sinusoidal input and output currents, bidirectional power flow capability and controllable input power factor, without using bulky energy storage elements.

In this thesis, different Pulse Width Modulation (PWM) strategies described in the literature are adapted to the proposed power converter topology. The issues of common-mode voltage and zero sequence voltage are reviewed and addressed with these modulation strategies.

The performance of the drive is tested via simulations in PSIM/MATLAB platform and experimentally verified with a laboratory prototype. Results for open and closed-loop operation of the system are presented and discussed.

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Chapter 1. Introduction

1.1. Background

Induction motors have been for years the most important electromechanical energy converter used in the industry because of their low cost, rugged construction and low maintenance requirements. When operated directly from the grid supply (50/60 Hz at essentially constant voltage), an induction motor operates at a nearly constant speed. Many motor applications, however, require several speeds or even a continuously adjustable range of speeds. Nowadays, by means of power electronic converters, it is possible to have flexible machine speed control. Static frequency converters have been largely used in Alternating Current (AC) industrial motor drives, in the last decades. These converters are typically controlled by Pulse Width Modulation (PWM) strategies and provide a simple and efficient way to control the speed of induction motors by varying the voltage and frequency supplied to them. However, despite the aforementioned advantages, some problems could arise when using PWM power converters in AC motor drives. One of these issues is the generation of high amplitude and frequency common-mode voltages. These voltages could cause undesirable circulating currents in the motor due to parasitic capacitances between the winding and the case [1]. These currents find their way via the motor bearings back to the grounded stator frame. The so-called bearing currents have been found to be a major cause of premature bearing failure in PWM inverter motor drives [2].

Different alternatives to reduce the effects of the common-mode voltage can be found in the technical literature, for instance the use of special filters, as proposed in [3]-[4], or the application of certain power converter configurations, as the conventional Neutral Point Clamped (NPC) three-level inverter, where only commutation states that do not produce common-mode voltage are used [5].

In the last years, dual-inverter systems feeding open-end winding induction motor drives have gained interest because they present several advantages when compared to a standard wye or delta connected induction machine drives. The main features of an open-winding induction machine drive can be summarized as [6]-[7]: each inverter is rated at half the machine power because power is supplied to the machine from both winding ends; each phase stator current can be controlled independently; possibility to have twice the effective switching frequency depending on the modulation strategy; extensibility to more phases leading to a phase current reduction; possibility of

reducing common-mode voltage; and certain degree of fault tolerance because of the voltage space vector redundancy.

However, an open-end winding induction machine drive can have some drawbacks, such as [6]: possibility of zero sequence current flowing in the machine because of the occurrence of zero sequence voltage when a single DC supply is used; increased conduction losses; higher complexity in the power converter, i.e. more power devices, circuit gate drives, etc.

The aim of this thesis is to study the application of an Indirect Matrix Converter (IMC) [8], with a dual-inverter output, to supply energy to an open-ended winding induction machine. Different PWM strategies are implemented for the proposed power converter topology. Two Space Vector Modulation (SVM) strategies are presented for the input rectifier stage of the IMC: one that maximizes the DC voltage and the other provides a reduced DC link voltage. For the output inverters, three modulation strategies are shown: a standard carrier-based PWM which achieves very low distorted input currents, a SVM that reduces the output phase zero sequence voltage and a SVM that reduces the common-mode voltage and compensate the low order zero sequence voltage.

The performance of the proposed open-end winding induction motor drive is verified via simulations in PSIM/MATLAB platform and experimentally verified with a 7.5 kW laboratory prototype. Results for open and closed-loop operation of the system are presented and discussed.

1.2. Literature Review

To support this thesis, several papers have been reviewed and separated into four main topics, depending on the power converter topology used to feed the machine: (1) Two two-level inverters fed by isolated DC sources, (2) Two two-level inverters fed by a single DC source, (3) Multilevel inverters and (4) Matrix converters. The articles will be briefly commented and a final discussion will be stated.

1.2.1 Two two-level inverters fed by isolated DC sources

This is the basic power converter for open-ended windings drives. The circuit configuration is shown in Fig. 1.1 where a standard two-level Voltage Source Inverter (VSI) is connected at each side of the machine stator winding. The VSIs are supplied by isolated DC power sources.

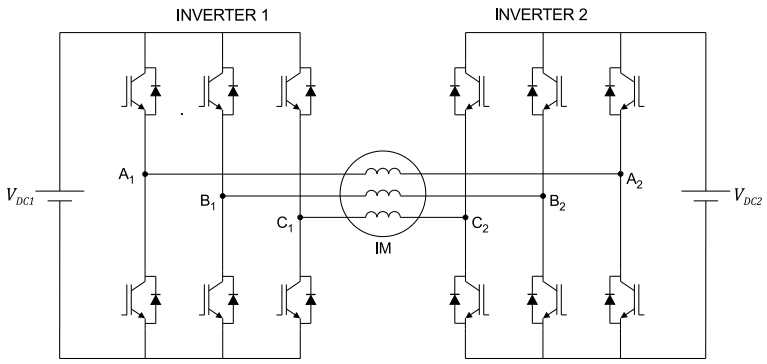


Fig. 1.1. Two 2-level VSIs fed by isolated DC sources for an open-end winding AC machine drive

Several papers have been published with the use of this circuit configuration. For instance [9] proposes a voltage harmonic suppression scheme for the dual-inverter, where selecting a specific magnitude ratio of the DC sources certain harmonic components of the machine phase voltage can be eliminated.

In [10], a random PWM technique for the system of Fig. 1.1 is presented. The output reference voltages of the inverters are compared to random carrier signals. This strategy achieves a reduction of the voltage harmonic content in comparison to the standard PWM based on a triangular carrier.

To reduce the switching losses of a dual-inverter, a Space Vector Modulation (SVM) strategy is presented in [11]. The strategy does not require sector identification and allows a reduction of 50% in the switching losses, in comparison to other dual-inverter PWM techniques where one inverter is clamped at a determined switching state while the other inverter commutates.

In [12], a scheme to obtain a four-level output phase voltage is proposed by using asymmetrical DC sources with magnitudes ratio of 2:1. A SVM strategy is also proposed for the drive.

A PWM strategy intended to reduce the current ripple in a dual two-level inverter topology is proposed in [13] and analytical approaches to predict the current trajectory and the ripple content of the open-end winding induction motor drive are presented in [14].

A passive filter to mitigate the effects of the common-mode voltage, such as the bearing currents is proposed in [15]. A PWM strategy that reduces the common-mode voltage of the open-end winding topology is presented in [16].

In [17], a comparative study between three different modulation strategies for open-ended windings AC machine drives is carried out. Simulation results are presented and the current ripple under each PWM method is analyzed.

The extension of the three-phase open-ended windings AC machine drive to multiphase machines is presented in [18]-[21] where different modulation strategies are presented and discussed. This extension is not straightforward because the number of possible switching states increases exponentially with the number of phases.

In general, the main characteristic of this topology is that circulation of zero sequence current in the machine windings is avoided; however it requires two isolation transformers to supply the DC sources, then increasing the cost and volume of drive.

1.2.2 Two two-level inverters fed by a single DC source

This topology is basically the same structure described in 1.2.1 but in this case only one DC supply is considered for the drive, as shown in Fig. 1.2. The main disadvantage of this converter is that zero sequence current could circulate though the machine windings due to the generation of output zero sequence voltage.

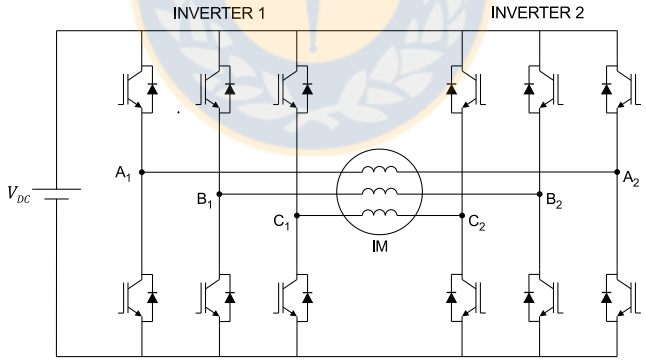


Fig. 1.2. Two 2-level VSIs fed by a single DC source for an open-end winding AC machine drive

To eliminate the occurrence of zero sequence currents in the machine windings, PWM strategies intended to eliminate the zero sequence voltage are proposed in [22]-[23]. In [24], a SVM strategy is proposed to dynamically compensate the zero sequence current by applying the null vectors with asymmetrical duty cycles in each switching period and in [25], the effect of the null-vector placement in the modulation for the dual-inverter system is thoroughly analyzed. On the other

hand, a closed-loop compensation scheme to suppress the zero sequence currents in the machine is developed in [26].

To obtain a common-mode voltage reduction, a SVM switching strategy is presented in [27]. This strategy uses only space vectors that do not produce common-mode voltage then reducing the problems associated to it such as the bearing currents.

A dual-inverter configuration fed by an active rectifier without DC link energy storage element (so-called direct-link converter) is presented in [28]-[29]; in [28], three modulation strategies are presented for the drive: a carrier-based PWM and two SVM strategies. In [29], common-mode voltage suppression is proposed and an active filter is added to the topology to inject compensating harmonic currents into the supply and allow controllable input power factor.

In [30]-[31] a PWM switching strategy aiming to reduce the zero sequence currents is presented, using auxiliary switches to provide a switched neutral. In this case, to the topology shown in Fig. 1.2, four auxiliary switches each consisting in one IGBT with four diodes are added, therefore increasing the cost, volume and complexity of the power converter but allowing more possible switching states. Finally, multiphase open-ended windings induction motor drives are presented in [32]-[35] where PWM techniques are proposed intended to reduce the common-mode voltage at the machine terminals; simulation and experimental results are shown.

1.2.3 Multilevel topologies

Several multilevel power converters have been developed for open-end winding induction motor drives. The main advantage of the multilevel topologies is that the machine phase voltage presents very low distortion then increasing the performance of the drive but on the other hand, the complexity and cost of the system is also increased.

Three-level inverter schemes based on cascaded two-level inverters are proposed in [36]-[39]. The converter presented in [36] requires a single DC source and the topologies shown in [37]-[39] consider two isolated DC supplies. In all these articles, PWM strategies aiming to reduce the common-mode voltage are presented.

Five-level power converter topologies for open-end winding AC drives are presented in [40]-[43]. In [40], a five-level machine phase voltage is achieved by connecting a three-level inverter at each side of the stator winding. The three-level inverters are supplied by isolated DC sources.

The five-level topology proposed in [41] is realized by cascading conventional two-level and three-level NPC inverters. A modulation strategy for common-mode voltage elimination is analyzed.

In [42], the five-level scheme consists on feeding one side of the stator winding with a three-level NPC inverter and the other side with a standard two-level VSI. Two isolated DC supplies are required. The circuit proposed in [43] considers supplying one end of the stator winding with a three-level inverter (based on two cascaded two-level VSIs) and the other end of the stator winding with a conventional two-level VSI. This topology uses three isolated DC supplies.

Higher number of voltage levels can be achieved with more complex power converter configurations [44]-[52]. These topologies allow having a very good quality machine phase voltage but the cost, volume and control complexity is increased resulting in a suitable solution just for high power medium voltage drives, where the advantages of the multilevel converters such as the enhanced quality of the output voltage at low switching frequencies, low electromagnetic interference, higher efficiency, etc., are very desirables.

1.2.4 Matrix converters

A Matrix Converter [53] is a direct frequency converter consisting on bidirectional switches allowing to connect any of the output terminals to any of the input voltages. For a three-phase open-end winding induction motor drive, two MCs are required, connected in the arrangement shown in Fig. 1.3. The main features of a matrix converter are: bidirectional power flow capability, sinusoidal input and output currents without bulky energy storage elements, and controllable input power factor. For the topology depicted in Fig. 1.3, it can be noted that a total of 36 IGBTs and diodes are required.

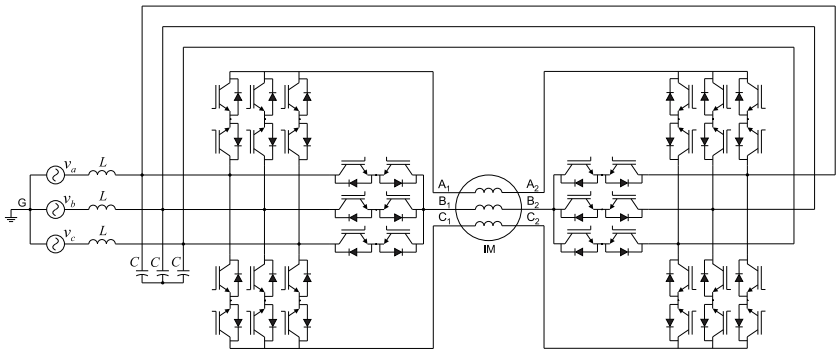


Fig. 1.3. Open-end winding induction motor drive based on matrix converters

The articles [54]-[58] consider the topology depicted in Fig. 1.3; in [54]-[56] the main features of the converter are described and a SVM strategy intended to reduce the common-mode voltage is presented. Simulation and experimental results are also shown. In [57]-[58] a thorough mathematical analysis of the power converter topology is carried out; a PWM strategy based on rotating space vector is considered.

Multiphase open-end winding induction machine drives based on dual matrix converter are presented in [59]-[62]. Analytical approaches to obtain the expression of the modulating signals that are used to generate the switching pulses for the matrix converters are discussed. A PWM algorithm aiming to eliminate the common-mode voltage is proposed.

A three-level indirect matrix converter topology to supply an open-end winding AC machine is presented in [63]. A detailed analysis of the PWM technique used for the proposed drive is shown. Furthermore, commutation strategies for the power devices of the presented drive are commented.

1.2.5 Comments

From the literature review, it can be appreciated that different power converter topologies have been proposed for open-end winding induction machine drives. Moreover, several modulation strategies with different goals are analyzed for the topologies presented. Many of the reviewed articles highlight the possibility of reducing the common-mode voltage in open-end winding AC motor drives. On the other hand, the disadvantage of eventual zero sequence current circulation when using a single DC source to feed a dual-inverter system is also commented.

Regarding open-end winding induction machine drives based on matrix converters, a few published papers can be found; furthermore, most of them are related to standard direct matrix converters. This is an important support to the originality of the research proposed in this thesis project, where the application of a two-output indirect matrix converter to supply an open-end winding induction motor is presented.

1.3. Project Objectives

1.3.1 General Objective

The main aim of this research work is to propose and verify the suitability of using an Indirect Matrix Converter with two output stages to supply energy to an open-end winding induction

machine.

1.3.2 Specific Objectives

- Implement and test two modulation strategies for the converter input rectifier:
  - SVM for maximum DC link voltage.
  - SVM for reduced DC link voltage.
- Implement and test three modulation strategies for the dual-inverter output:
  - Carrier-based PWM.
  - SVM for zero sequence voltage reduction.
  - SVM for common-mode voltage reduction.
- Implement a vector control strategy for the machine currents.
- Simulate the modulation and control strategies in PSIM/MATLAB platform
- Verify the proposal in a 7.5 kW laboratory prototype.

1.4. Thesis overview

The present thesis is organized as follows. In Chapter 2 a full description of the open-end winding machine drive based on a two-output IMC is presented. This includes a mathematical model of the drive and the calculation of the converter voltage gain. Moreover the issues of zero sequence and common-mode voltages present in an open-end winding topology are discussed and the guidelines to reduce them are also stated.

Chapter 3 presents different modulation strategies for the power converter. Two SVM strategies for the input rectifier are shown: one produces a reduced DC voltage and the other maximizes the DC link voltage. For the converter output stages three PWM strategies are presented; a carrier-based modulation that produces a very low distorted input currents and two SVM strategies intended to reduce the zero sequence and/or the common-mode voltages.

Chapter 4 covers the description of the experimental system implemented to verify the performance of the modulation strategies proposed for the open-end winding machine drive. The details of the power converter construction and the control platforms are given in this chapter.

Moreover, the specifications of the induction machine used and the voltage/current measuring transducers are also stated in Chapter 4.

Simulation and experimental results obtained for the open-end winding topology are presented in Chapter 5. The performance of the modulation strategies presented in Chapter 3 is verified for open and closed-loop operation of the machine and the results are shown and discussed.

Finally Chapter 6 presents the overall conclusions of this thesis project and highlights the conference and journal publications obtained with the carried out research.

Chapter 2. Power converter topology and machine modelling

This chapter describes the open-end winding induction machine and the Indirect Matrix Converter (IMC) models. The voltage gain of the dual-output IMC is derived. The issues related to zero sequence voltage and common-mode voltage present in an open-end winding connected machine are addressed and analyzed.

2.1. Introduction

An IMC, see Fig. 2.1, is an AC/AC frequency converter which provides similar features as a standard Matrix Converter (MC), which are [53]:

- Four-quadrant operation.
- Sinusoidal input currents.
- No bulky energy storage elements.
- Controllable input power factor.

On the other hand, among the main disadvantages of an IMC, the following can be mentioned [53]:

- Theoretical converter voltage gain of 86 %.
- Low immunity to external perturbation.
- Lack of ride-through capability.
- High number of power devices.

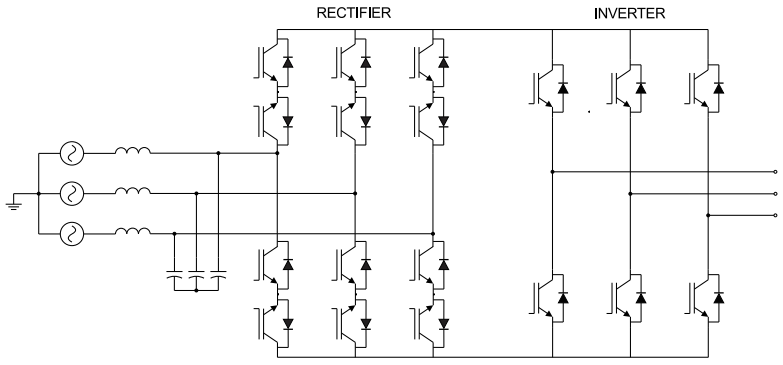


Fig. 2.1. Standard indirect matrix converter

As shown in Fig. 2.1, the IMC considers two power stages, rectifier and inverter, allowing certain degree of independent control for both. Having two separate stages makes the IMC a more flexible and reliable alternative than the MC [8], i.e. multiple input stages and/or multiple output stages are feasible.

MCs and IMCs have been widely studied for several years and proposed as a suitable solution for loads requiring fixed/variable voltage and frequency in systems where the volume and weight of the power converter is critical.

2.2. Open-end winding induction motor drive based on IMC

If an open-end winding induction machine is to be supplied by an IMC, a second VSI output needs to be added to the circuit configuration of Fig. 2.1. The resulting power converter topology is shown in Fig. 2.2, where the input rectifier provides the DC voltage to the dual-inverter system outputs. The six induction machine open-end windings are connected between the two VSI outputs. As can be noted in Fig. 2.2, considering the six bidirectional switches of the input stage and the two output stages, a total of 24 discrete IGBTs and diodes are needed in this topology. That is an advantage in comparison to the open-end winding topology based on MCs, where 36 IGBTs and diodes are required [56].

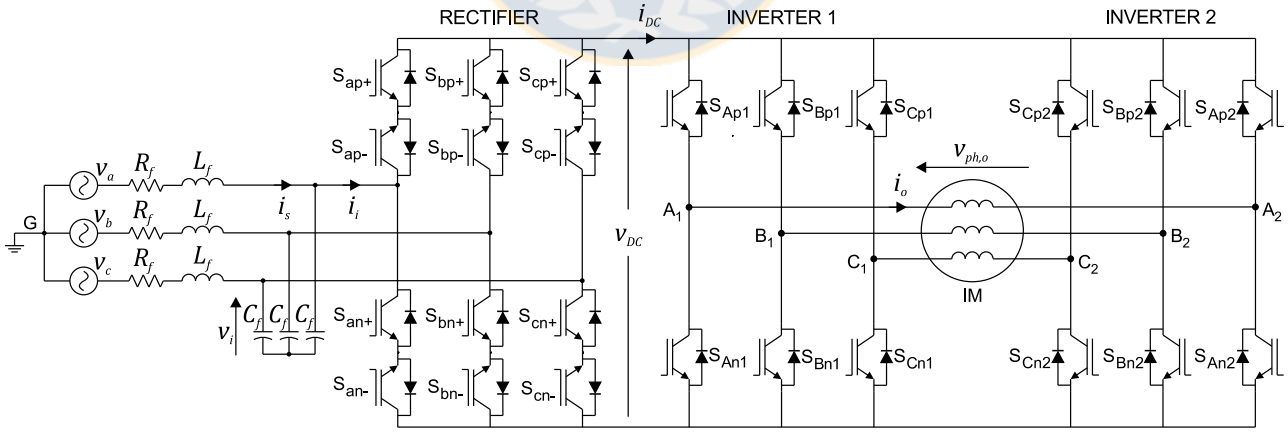


Fig. 2.2. Open-end winding induction machine fed by a two-output IMC

The three voltages produced by both output stages of the IMC are depicted in Fig. 2.3. These voltages are measured with respect to a virtual midpoint of the DC link. Then it is possible to calculate the sum of the voltage vectors:

$$\underline{v}_{sum} = \underline{v}_{A1} + \underline{v}_{B1} + \underline{v}_{C1} + \underline{v}_{A2} + \underline{v}_{B2} + \underline{v}_{C2} \tag{2.1}$$

$$\underline{v}_{sum} = v_{A1}e^{j0} + v_{B1}e^{-j\frac{2\pi}{3}} + v_{C1}e^{j\frac{2\pi}{3}} + v_{A2}e^{j\pi} + v_{B2}e^{j\frac{\pi}{3}} + v_{C2}e^{-j\frac{\pi}{3}} \tag{2.2}$$

Using the Euler's formula, $e^{j\alpha} = \cos\alpha + j\sin\alpha$, it is obtained:

$$\underline{v}_{sum} = \left[v_{A1} - v_{A2} - \frac{1}{2}(v_{B1} - v_{B2}) - \frac{1}{2}(v_{C1} - v_{C2})\right] + j\frac{\sqrt{3}}{2}[-v_{B1} + v_{B2} + v_{C1} - v_{C2}] \tag{2.3}$$

that can be rewritten as:

$$\underline{v}_{sum} = \left(v_{A1A2} - \frac{1}{2}v_{B1B2} - \frac{1}{2}v_{C1C2}\right) + j\frac{\sqrt{3}}{2}(v_{C1C2} - v_{B1B2}) \tag{2.4}$$

Finally, the output voltage space vector can be defined as:

$$\underline{v}_o = \frac{2}{3}\underline{v}_{sum} = \frac{2}{3}\left(v_{A1A2} + v_{B1B2}e^{-j\frac{2\pi}{3}} + v_{C1C2}e^{j\frac{2\pi}{3}}\right) = v_o e^{j\theta} \tag{2.5}$$

where v_o is the magnitude and θ the angle of the space vector. The coefficient $2/3$ is a scaling factor that has been added to keep constant magnitude of the vectors during the transformation [64].

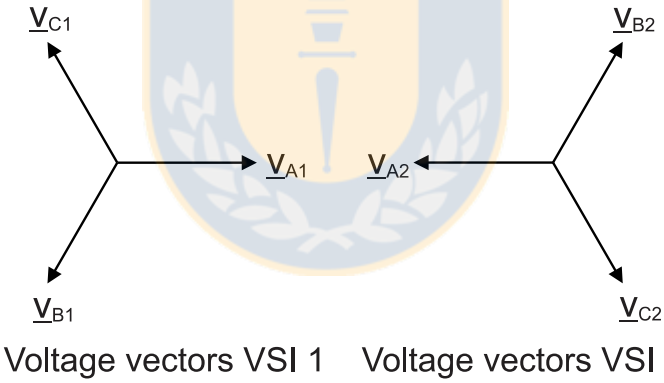


Fig. 2.3. Voltages vectors of the individual inverters

Regarding the output stages of the IMC, each inverter can produce eight independent voltage space vectors. Thus, there are a total of 64 vector combinations for the dual-inverter system, resulting in a space vector locus similar to a three-level Neutral Point Clamped (NPC) inverter [10]. The space vectors for inverter 1 are shown in Table 2.1; the same space vectors are valid for inverter 2 but with superscript 2. A representation of the individual inverters space vectors is shown in Fig. 2.4.

Let $V_{ij} = [V_i^1 V_j^2]$ with $i, j = 1 \ldots 8$, be the phase voltage vector combination of the dual-inverter output, hence a diagram of the vector locations is shown in Fig. 2.5 [10] where the

availability of redundant switching states for some voltage space vectors of the dual-inverter can be appreciated. This diagram is obtained by carrying out the vector sum of all the possible space vector combinations of inverters 1 and 2 (Fig. 2.4).

Table 2.1. Switching states of the individual inverter

States of inverter 1 $[S_{A1}\ S_{B1}\ S_{C1}]$			
$V_1^1 = [1\ 0\ 0]$	$V_2^1 = [1\ 1\ 0]$	$V_3^1 = [0\ 1\ 0]$	$V_4^1 = [0\ 1\ 1]$
$V_5^1 = [0\ 0\ 1]$	$V_6^1 = [1\ 0\ 1]$	$V_7^1 = [1\ 1\ 1]$	$V_8^1 = [0\ 0\ 0]$

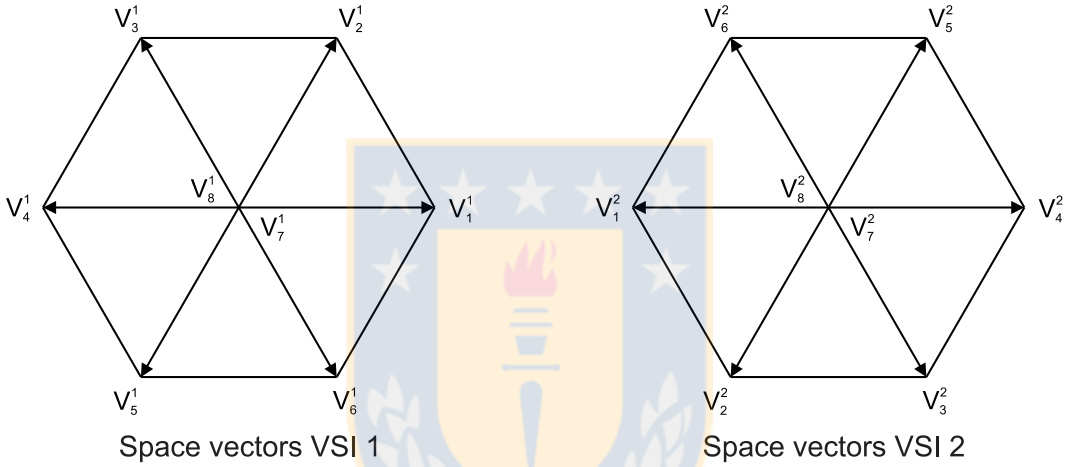


Fig. 2.4. Space vectors representation of the individual inverters

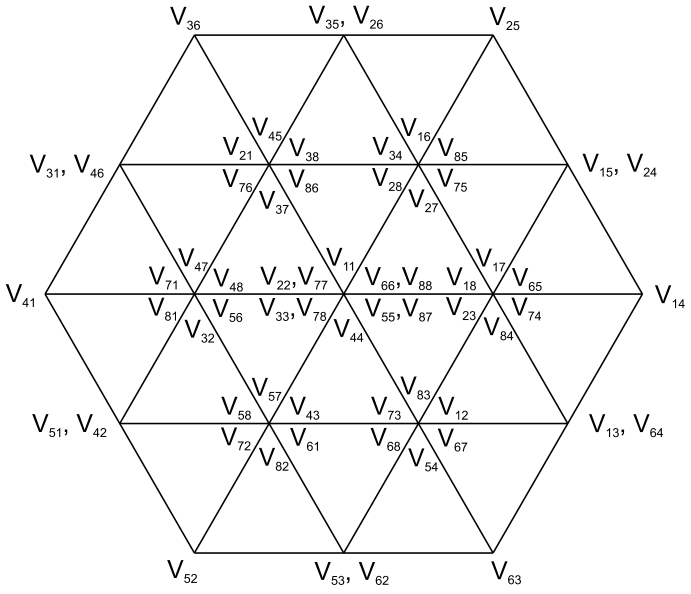


Fig. 2.5. Space vector locations of the dual-inverter scheme

The magnitude of the active space voltage vectors can be calculated considering that each machine phase winding can be supplied with a voltage of $-V_{DC}$, 0 or $+V_{DC}$. For instance, the vector V_{14} applies $+V_{DC}$ to the machine phase-a winding and $-V_{DC}$ to the machine phase b and c windings. This results in:

$$\underline{V}_{14} = V_{DC} - V_{DC}e^{-j\frac{2\pi}{3}} - V_{DC}e^{j\frac{2\pi}{3}} = 2V_{DC}\angle 0° \; [V] \tag{2.6}$$

The same procedure can be used to calculate the magnitude of each active space voltage vector of the dual-inverter system. This is summarized in Table 2.2.

Table 2.2. Magnitude of the dual-inverter active space vectors

	Space Vectors	Magnitude
Largest	$V_{14}, V_{25}, V_{36}, V_{41}, V_{52}, V_{63}$	$2V_{DC}$
Medium	$V_{15}, V_{24}, V_{35}, V_{26}, V_{31}, V_{46}, V_{51}, V_{42}, V_{53}, V_{62}, V_{13}, V_{64}$	$\sqrt{3}V_{DC}$
Lowest	$V_{65}, V_{17}, V_{18}, V_{23}, V_{84}, V_{74}, V_{85}, V_{16}, V_{34}, V_{28}, V_{27}, V_{75}$ $V_{38}, V_{45}, V_{21}, V_{76}, V_{37}, V_{86}, V_{48}, V_{47}, V_{71}, V_{81}, V_{32}, V_{56}$ $V_{43}, V_{57}, V_{58}, V_{72}, V_{82}, V_{61}, V_{12}, V_{83}, V_{73}, V_{68}, V_{54}, V_{67}$	V_{DC}

As can be noted from Table 2.2 and Fig. 2.5, the six largest vectors have a magnitude of twice the DC link voltage and have no redundancy. On the other hand, the higher redundancy is present for the lowest vectors each having six switching states available to produce the same output voltage.

2.3. Commutation of bidirectional switches

To commutate bidirectional switches, such as the common-emitter configuration shown in Fig. 2.6 (used in the rectifier of the topology depicted in Fig. 2.2), the four-step commutation method is used. This commutation method can be controlled either by the sign (direction) of the output current or the sign of the input line voltage. The main objective of this method is to avoid short circuit and/or open circuit conditions in the converter output (the DC link in the power converter of Fig. 2.2).

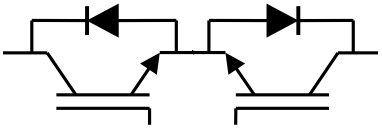


Fig. 2.6. Bidirectional switch (common-emitter)

To illustrate the four-step commutation method, Fig. 2.7 shows a circuit consisting of two bidirectional switches. Initially, the load is connected to phase-a (switch S_a closed) and a commutation to phase-b is required. Depending on the commutation method used (controlled by output current or input voltage sign), the switching process will be different and is described in sections 2.3.1 and 2.3.2.

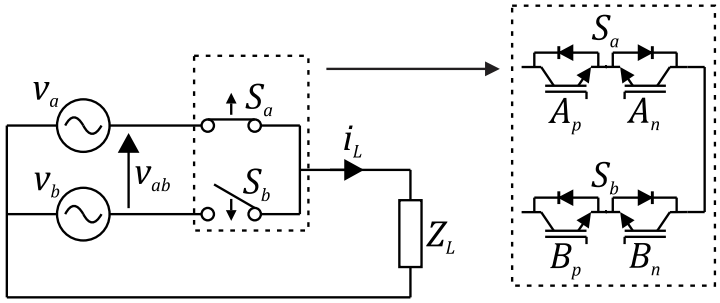


Fig. 2.7. Circuit with two bidirectional switches

2.3.1 Commutation controlled by output current sign

For this strategy the order of the commutation process to connect the load of Fig. 2.7 to phase-b is shown in the diagrams of Fig. 2.8. In this case, when the output current I_L is positive (→) and the switches A_p-A_n are closed and the switches B_p-B_n are opened, the commutation process can initiate by turning off the switch is not conducting A_n. Then, the switch B_p can be turned on without short circuiting the input phases, since A_n and B_n are opened. The process continues turning off the switch A_p as in the previous step a current circulation path has been provided, avoiding an open circuit of the load. Finally, switch B_n is turned on and the commutation process from phase-a to phase-b is over.

2.3.2 Commutation controlled by input voltage sign

For this strategy the order of the commutation process to connect the load of Fig. 2.7 to phase-b is shown in the diagram of Fig. 2.9. In this case, when the voltage V_{ab} is positive ($V_a > V_b$) with the switches A_p-A_n closed and the switches B_p-B_n opened, the commutation process can initiate by turning on the switch B_p, avoiding a short circuit of the input phases. Then, the switch A_p can be turned off with no effect on the load current which circulates through B_p. The process continues turning on the switch B_n without short circuiting the input phases since A_p is opened. Finally, the switch A_n can be turned off ending the commutation process.

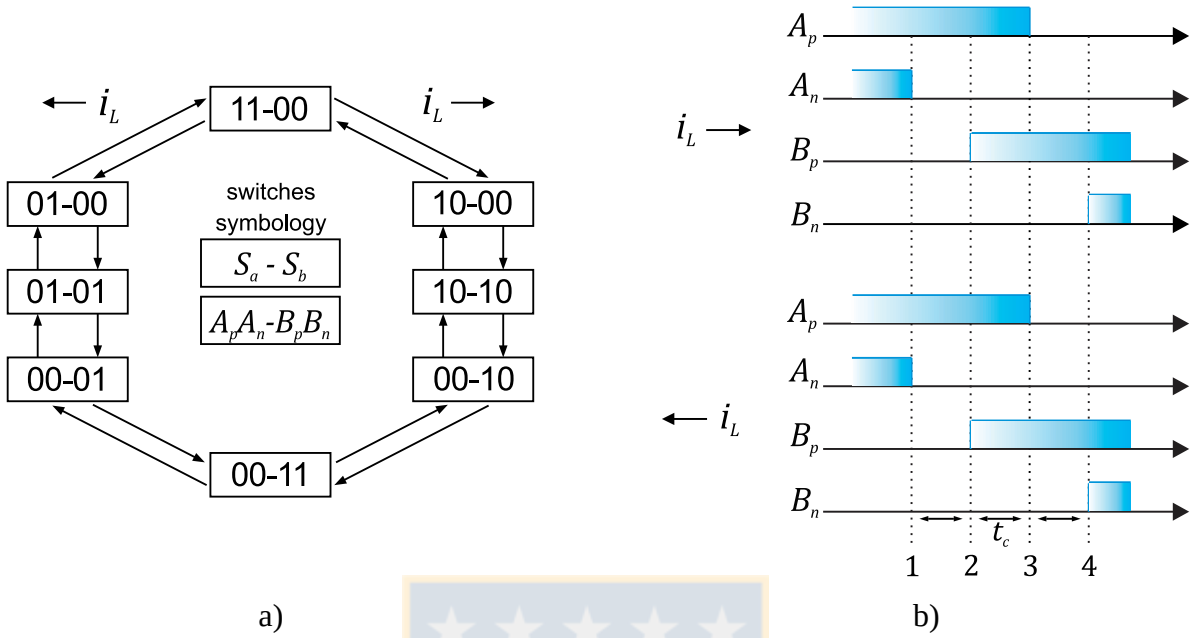


Fig. 2.8. Current-controlled commutation process. a) Switching states and b) Gate signals of the power devices (t_c: commutation time)

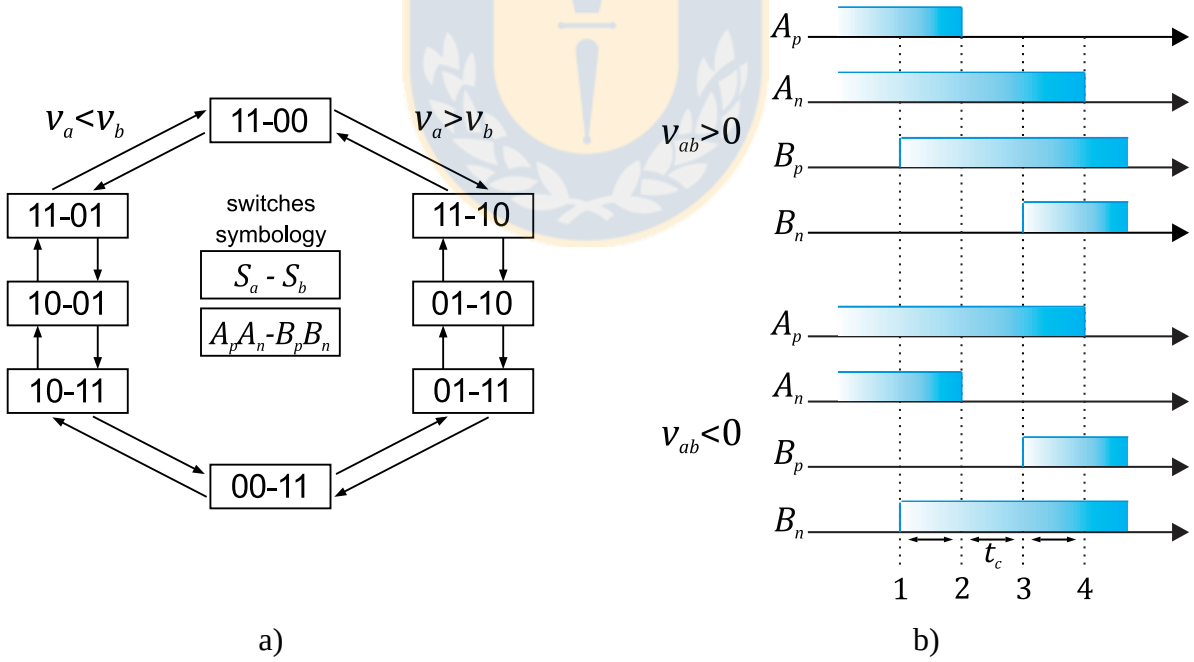


Fig. 2.9. Voltage-controlled commutation process. a) Switching states and b) Gate signals of the power devices (t_c: commutation time)

For matrix converters, the method is controlled by the sign of the output current. However, as the DC link current of the indirect matrix converter used in topology proposed (Fig. 2.2) is

discontinuous, the commutation of the rectifier input stage used in this work is based on the sign of the input line voltage.

2.4. Power converter voltage gain

The input rectifier of an IMC is usually modulated to maximize the DC link voltage [65]. However, due to the absence of a bulky capacitor in the converter DC link, the average value of the DC voltage will vary between a minimum $V_{pn,min} = \frac{\sqrt{3}}{2}\hat{V}_{s,l-l}$ and a maximum $V_{pn,max} = \hat{V}_{s,l-l}$, where $\hat{V}_{s,l-l}$ is the peak value of the input line-to-line voltage [65]-[66]. The output voltage vector locus is shown in Fig. 2.10 where the blue dashed hexagon represents the average DC link voltage.

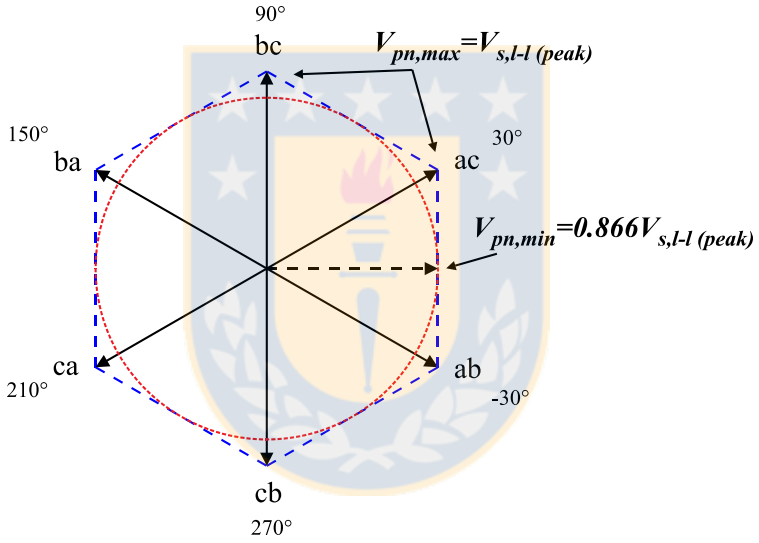


Fig. 2.10. Output voltage vector locus for the average DC link voltage

The voltage produced by the output stages is then limited by the minimum average DC voltage (red circle in Fig. 2.10). As each machine phase winding can be considered to be supplied by a standard H-bridge inverter, the amplitude of the fundamental frequency output phase voltage is given by [67]:

$$\hat{V}_{o,ph} = m_o V_{pn,min} = m_o \frac{\sqrt{3}}{2}\hat{V}_{s,l-l} \tag{2.7}$$

where m_o is a modulation index for the output inverters ($0 \leq m_o \leq 1$). Since the input phase voltage equals $\sqrt{3}$ times the input line voltage, eq. (2.7) can be rewritten as:

$$\hat{V}_{o,ph} = m_o \frac{\sqrt{3}}{2} \sqrt{3} \hat{V}_{s,ph} = 1.5 m_o \hat{V}_{s,ph} \tag{2.8}$$

where $\hat{V}_{s,ph}$ is the peak value of the input phase voltage. Hence, the proposed topology is capable to generate a maximum output phase voltage of 1.5 times the input phase voltage, without over-modulation.

2.5. Power converter and machine model

The complete drive shown in Fig. 2.2 can be modeled by state equations which describe the dynamic behavior of the system. The converter power devices are considered ideal, then commutation times and voltage drops in semiconductors are neglected. The state variables of the system are (see Fig. 2.2) the source current $\boldsymbol{i_s}$, the converter input voltage $\boldsymbol{v_i}$, the output current $\boldsymbol{i_o}$, the mechanical rotor speed ω_r and the rotor angle θ_r. Since the model will be derived in fixed *abc* coordinate frame, the electrical state variables can be written as follows:

$$\boldsymbol{i_s} = [i_{sa} \quad i_{sb} \quad i_{sc}]^T, \boldsymbol{v_i} = [v_{ia} \quad v_{ib} \quad v_{ic}]^T, \boldsymbol{i_o} = [i_{oa} \quad i_{ob} \quad i_{oc}]^T \tag{2.9}$$

The differential equations for the input side are:

$$\boldsymbol{v_s} = R_f \boldsymbol{i_s} + L_f \frac{d\boldsymbol{i_s}}{dt} + \boldsymbol{v_i} \tag{2.10}$$

$$\boldsymbol{i_s} = C_f \frac{d\boldsymbol{v_i}}{dt} + \boldsymbol{i_i} \tag{2.11}$$

where $\boldsymbol{v_s}$ is the source voltage and $\boldsymbol{i_i}$ is the rectifier input current:

$$\boldsymbol{v_s} = [v_{sa} \quad v_{sb} \quad v_{sc}]^T, \boldsymbol{i_i} = [i_{ia} \quad i_{ib} \quad i_{ic}]^T \tag{2.12}$$

The DC link voltage v_{DC} can be obtained as:

$$v_{DC} = \boldsymbol{S_r^T} \cdot \boldsymbol{v_i} \tag{2.13}$$

with the rectifier switching matrix:

$$\boldsymbol{S_r} = \begin{bmatrix} S_{ap} - S_{an} \\ S_{bp} - S_{bn} \\ S_{cp} - S_{cn} \end{bmatrix} \tag{2.14}$$

where $S_{xp}, S_{xn} \in \{0,1\}$ with $x = a, b, c$. The output pole voltage of Inverter 1 ($\boldsymbol{v_{o1}}$) and Inverter 2 ($\boldsymbol{v_{o2}}$) respect to the negative DC link rail, are defined by:

$$\boldsymbol{v_{o1}} = \boldsymbol{S_{i1}} \cdot v_{DC}, \boldsymbol{v_{o2}} = \boldsymbol{S_{i2}} \cdot v_{DC} \tag{2.15}$$

where the switching matrices of Inverter 1 ($\boldsymbol{S_{i1}}$) and Inverter 2 ($\boldsymbol{S_{i2}}$) are:

$$\boldsymbol{S_{i1}} = \begin{bmatrix} S_{A1} \\ S_{B1} \\ S_{C1} \end{bmatrix} = \begin{bmatrix} S_{Ap1} - S_{An1} \\ S_{Bp1} - S_{Bn1} \\ S_{Cp1} - S_{Cn1} \end{bmatrix}, \boldsymbol{S_{i2}} = \begin{bmatrix} S_{A2} \\ S_{B2} \\ S_{C2} \end{bmatrix} = \begin{bmatrix} S_{Ap2} - S_{An2} \\ S_{Bp2} - S_{Bn2} \\ S_{Cp2} - S_{Cn2} \end{bmatrix} \tag{2.16}$$

and $S_{xpk} = \bar{S}_{xnk} \in \{0,1\}$ with $x = a, b, c$, $k = 1,2$. The output phase voltages correspond to the pole voltage difference of both inverters:

$$\boldsymbol{v_{ph,o}} = [v_{ph,oa} \quad v_{ph,ob} \quad v_{ph,oc}]^T = \boldsymbol{v_{o1}} - \boldsymbol{v_{o2}} = (\boldsymbol{S_{i1}} - \boldsymbol{S_{i2}}) v_{DC} \tag{2.17}$$

Considering a model of the AC machine with R_s the stator resistance, the output phase voltage can be written as:

$$\boldsymbol{v_{ph,o}} = R_s \boldsymbol{i_o} + \frac{d\boldsymbol{\Psi_s}(\boldsymbol{i_o}, \boldsymbol{i_r}, \theta_r)}{dt} \tag{2.18}$$

where $\boldsymbol{\Psi_s}$ is the stator flux linkage and $\boldsymbol{i_r}$ is the rotor current given by:

$$\boldsymbol{\Psi_s} = [\Psi_{sa} \quad \Psi_{sb} \quad \Psi_{sc}]^T, \boldsymbol{i_r} = [i_{ra} \quad i_{rb} \quad i_{rc}]^T \tag{2.19}$$

As $\boldsymbol{\Psi_s}$ is a implicit function of t, (2.18) can be rewritten by using the chain rule for the derivative:

$$\boldsymbol{v_{ph,o}} = R_s \boldsymbol{i_o} + \frac{\partial \boldsymbol{\Psi_s}}{\partial \boldsymbol{i_o}} \frac{d\boldsymbol{i_o}}{dt} + \boldsymbol{\psi_2}(t) \tag{2.20}$$

where

$$\boldsymbol{\psi_2}(t) = \frac{\partial \boldsymbol{\Psi_s}}{\partial \boldsymbol{i_r}} \frac{d\boldsymbol{i_r}}{dt} + \frac{\partial \boldsymbol{\Psi_s}}{\partial \theta_r} \frac{d\theta_r}{dt} \tag{2.21}$$

Assuming $\partial \boldsymbol{\Psi_s} / \partial \boldsymbol{i_o}$ is a bijective function of t, it can be defined as:

$$\frac{\partial \boldsymbol{\Psi_s}}{\partial \boldsymbol{i_o}} = \boldsymbol{\psi_1^{-1}}(t) \tag{2.22}$$

and (2.20) can be redefined by:

$$\boldsymbol{v_{ph,o}} = R_s \boldsymbol{i_o} + \boldsymbol{\psi_1^{-1}}(t) \frac{d\boldsymbol{i_o}}{dt} + \boldsymbol{\psi_2}(t) \tag{2.23}$$

The DC link current is:

$$i_{DC} = (\boldsymbol{S_{i1}} + \boldsymbol{S_{i2}})^T \boldsymbol{i_o} \tag{2.24}$$

and the rectifier input current:

$$\boldsymbol{i_i} = \boldsymbol{S_r} i_{DC} \tag{2.25}$$

Defining the rotor flux vector $\boldsymbol{\Psi_r} = [\Psi_{ra} \quad \Psi_{rb} \quad \Psi_{rc}]^T$, the rotor inertia J_m, the motor viscous friction coefficient B_m, the torque produced by the motor T and the load torque T_L, the state space model of the drive is given by:

$$\frac{d\boldsymbol{i_s}}{dt} = -\frac{R_f}{L_f}\boldsymbol{i_s} - \frac{1}{L_f}\boldsymbol{v_i} + \frac{1}{L_f}\boldsymbol{v_s} \tag{2.26}$$

$$\frac{d\boldsymbol{v_i}}{dt} = \frac{1}{C_f}\boldsymbol{i_s} - \frac{1}{C_f}\boldsymbol{S_r}(\boldsymbol{S_{i1}} + \boldsymbol{S_{i2}})^T\boldsymbol{i_o} \tag{2.27}$$

$$\frac{d\boldsymbol{i_o}}{dt} = -\boldsymbol{\psi_1}(t)R_s\boldsymbol{i_o} - \boldsymbol{\psi_1}(t)\boldsymbol{\psi_2}(t) + \boldsymbol{\psi_1}(t)(\boldsymbol{S_{i1}} - \boldsymbol{S_{i2}})\boldsymbol{S_r^T} \cdot \boldsymbol{v_i} \tag{2.28}$$

$$T = K|\boldsymbol{i_s}||\boldsymbol{\Psi_r}|\sin\theta \tag{2.29}$$

$$T = J_m\frac{d\omega_r}{dt} + B_m\omega_r + T_L \tag{2.30}$$

$$\omega_r = \frac{d\theta_r}{dt} \tag{2.31}$$

where K is a constant depending on constructive characteristics of the machine and θ is the angle between the vectors $\boldsymbol{i_s}$ and $\boldsymbol{\Psi_r}$. Both θ and ω_r are measured in electric radians and rad/s, respectively.

The derived mathematical model of the open-end winding induction motor drive fed by an IMC will be used for simulation purposes and the design of the current control controllers for the vector ontrol application described in Chapter 5.

2.6. Zero sequence voltage

2.6.1 Introduction

It is well known that unbalanced three-phase voltages (or currents) can be transformed into three sets of voltage components [68]. These so-called symmetrical components are known as positive, negative and zero sequence components and can be schematically represented as shown in Fig. 2.11a. Positive and negative sequence components correspond to three-phase balanced rotating phasors and zero sequence components are phasors with zero phase shift angle. Fig. 2.11b shows a decomposition of an unbalanced three-phase voltage into symmetrical voltage components.

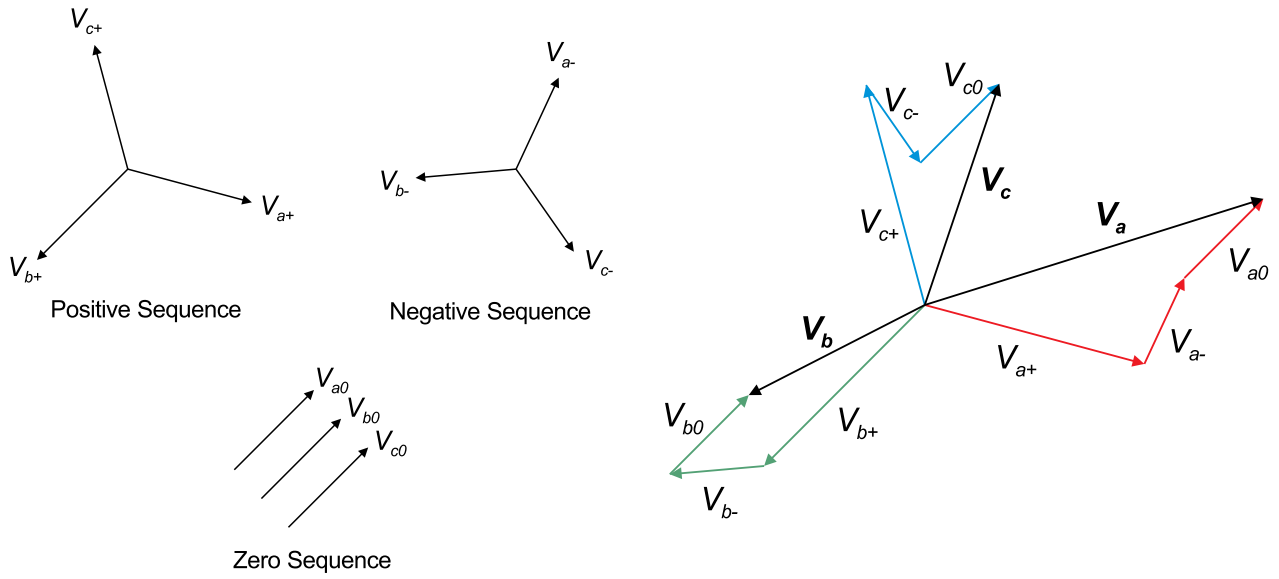


Fig. 2.11. a) Symmetrical components. b) Decomposition of unbalanced three-phase voltage into symmetrical components

Unlike the positive and negative sequence currents, the main issue of the zero sequence currents is that they do not cancel but add up arithmetically at the neutral point of a four wire three-phase system, eventually overloading the neutral line or producing a higher neutral to ground voltage. Additionally, harmonic currents of any sequence circulating in an AC drive may give rise to increased RMS current, thus increasing the system losses; high current/voltage THD and machine over-heating and vibrations.

2.6.2 Zero sequence voltage in open-end winding machine drive based on IMC

An open-end winding induction motor drive supplied by a dual-inverter with a single DC source may suffer from zero sequence current caused by zero sequence voltage. This zero sequence voltage is produced because of the asymmetry of the instantaneous pulse width modulated phase voltages applied to the machine windings (due to the voltage space vectors used). The zero sequence voltage is given by [24]:

$$v_{zs} = \frac{v_{A1A2} + v_{B1B2} + v_{C1C2}}{3} \tag{2.32}$$

or in terms of (2.17):

$$v_{zs} = \frac{1}{3}\sum_{k=a,b,c} v_{ph,ok} = \frac{v_{DC}}{3}\sum_{k=A,B,C}(S_{k1} - S_{k2}) \tag{2.33}$$

Thus, in order to make $v_{zs} = 0$, the following relationship must be satisfied:

$$\sum_{k=A,B,C} S_{k1} = \sum_{k=A,B,C} S_{k2} \tag{2.34}$$

Therefore, to eliminate the instantaneous zero sequence voltage in the load is necessary and sufficient to have the same number of upper (or lower) switches closed on both output inverters at every switching period.

On the other hand, if (2.13) is considered, v_{zs} can be rewritten as:

$$v_{zs} = \frac{1}{3}\boldsymbol{S_r^T} \cdot \boldsymbol{v_i} \sum_{k=A,B,C} (S_{k1} - S_{k2}) \tag{2.35}$$

$$v_{zs} = \frac{1}{3}\begin{bmatrix} S_{ap} - S_{an} \\ S_{bp} - S_{bn} \\ S_{cp} - S_{cn} \end{bmatrix}^T \begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix} \sum_{k=A,B,C} (S_{k1} - S_{k2}) \tag{2.36}$$

where $\boldsymbol{S_r}$ is the rectifier switching matrix and $\boldsymbol{v_i}$ is the input voltage vector. It can be noted in (2.36) that the switching strategy for the input stage of the IMC does affect the magnitude of the zero sequence voltage produced by the output stages but does not allow to make v_{zs} equal zero (unless all the rectifier switches were turned ON or OFF which neither useful nor permissible state).

By using (2.32), the zero sequence voltage contribution from the 64 space vector combinations of the dual-inverter topology can be calculated and are shown in Table 2.3. As can be noted, there are twenty space voltage vectors that do not produce zero sequence voltage, thus satisfying (2.34). Hence, in order to avoid the circulation of zero sequence current in the machine windings only these space voltage vector combinations could be used in the modulation strategy for the dual-inverter [28].

Moreover, from Table 2.3 and Fig. 2.5 it can be noted that there are two different but equivalent sets of active voltage vectors producing null zero sequence voltage (see Table 2.4), which could be used along with the zero voltage vectors: V_{11}, V_{22}, V_{33}, V_{44}, V_{55}, V_{66}, V_{77} and V_{88}.

Table 2.3. Zero sequence voltage contributions from different space vector combinations

V_{zs}	Voltage vector combinations
$-V_{DC}/2$	V_{87}
$-V_{DC}/3$	$V_{84}, V_{86}, V_{82}, V_{57}, V_{37}, V_{17}$
$-V_{DC}/6$	$V_{85}, V_{83}, V_{54}, V_{34}, V_{81}, V_{56}, V_{52}, V_{36}$ $V_{32}, V_{47}, V_{14}, V_{16}, V_{12}, V_{67}, V_{27}$
0	$V_{88}, V_{55}, V_{53}, V_{35}, V_{33}, V_{44}, V_{51}, V_{31}, V_{46}, V_{42}$ $V_{15}, V_{13}, V_{64}, V_{24}, V_{11}, V_{66}, V_{62}, V_{26}, V_{22}, V_{77}$
$+V_{DC}/6$	$V_{58}, V_{38}, V_{45}, V_{43}, V_{18}, V_{65}, V_{25}, V_{63}$ $V_{23}, V_{74}, V_{41}, V_{61}, V_{21}, V_{76}, V_{72}$
$+V_{DC}/3$	$V_{48}, V_{68}, V_{82}, V_{75}, V_{73}, V_{71}$
$+V_{DC}/2$	V_{78}

Table 2.4. Active space vectors producing null zero sequence voltage

Set 1	V_{15}	V_{35}	V_{31}	V_{51}	V_{53}	V_{13}
Set 2	V_{24}	V_{26}	V_{46}	V_{42}	V_{62}	V_{64}

Besides the use of space voltage vectors producing null v_{zs}, the occurrence of low order triplen harmonics in the machine currents could be avoided performing a dynamic balance for the zero sequence current as proposed in [24]. This dynamic compensation method will be further discussed in chapter 3.

2.7. Common-mode voltage

2.7.1 Introduction

A typical three-phase sinusoidal power supply is balanced and symmetrical under normal conditions; that is, the sum of the three instantaneous voltages is zero. Thus, when supplying a balanced three-phase load, the voltage between an equivalent neutral point of the load and the neutral point of the voltage source is zero. Usually the neutral point of the power source is grounded.

On the other hand, a three-phase PWM inverter is a source of asymmetrical voltages that switches a DC bus voltage (V_{DC}) onto the three phase terminals of the load, with a switching pattern that generates the proper fundamental frequency output voltage [67]. Since the output pole voltage of a two-level inverter, with respect to the negative rail of the DC bus, can be either $+V_{DC}$ or zero, it

is not possible to have the three terminal voltages added to zero at any instant of time. The average voltage applied to the motor (over a cycle) is kept zero, but the instantaneous sum of the voltages at the load terminals is nonzero. Then, a voltage will appear between an equivalent neutral point of the load and the electrical ground of the system. This voltage is called common-mode voltage [69].

In an open-end winding machine, such as depicted in Fig. 2.2, the common-mode voltage is given by [27]:

$$v_{cm} = \frac{1}{6}(v_{A1G} + v_{B1G} + v_{C1G} + v_{A2G} + v_{B2G} + v_{C2G}) \tag{2.37}$$

where v_{AiG}, v_{BiG}, v_{CiG}, with $i = 1,2$, are the pole voltages of each inverter with respect to the grounded neutral point of the power source (Fig. 2.2).

Because of the typically high switching frequency of a PWM inverter is in the kHz range, the common-mode voltage has a high rate of change with respect to time (high dV/dt) and will generate common-mode currents due to capacitive couplings ($I_{cm} = C\, dV/dt$). Moreover, higher inverter switching frequencies will originate higher common-mode currents.

The capacitive couplings between different parts of a machine originate many potential paths for these common-mode currents to flow. The most common paths are [70]: stator to rotor, stator winding to frame, rotor to shaft and shaft to frame. Therefore, it is possible the circulation of common-mode currents via the motor bearings back to the grounded stator case. The so-called bearing currents have been found to be a major cause of premature bearing failure in PWM inverter motor drives [70]. Thus a common-mode voltage reduction has been a topic of interest for many years.

2.7.2 Common-mode voltage reduction

One of the main advantages of an open-end winding machine connection is that allows the possibility of reducing the common-mode voltage then reducing the problems associated to it .

In the power converter topology shown in Fig. 2.2, the pole voltages v_{AiG}, v_{BiG}, v_{CiG}, with $i = 1,2$, can be expressed as:

$$\begin{aligned} v_{AiG} &= S_{Api}v_{pG} + S_{Ani}v_{nG} \\ v_{BiG} &= S_{Bpi}v_{pG} + S_{Bni}v_{nG} \\ v_{CiG} &= S_{Cpi}v_{pG} + S_{Cni}v_{nG} \end{aligned} \tag{2.38}$$

where v_{pG} and v_{nG} are the voltages of the positive and negative rail of the DC link with respect to the grounded neutral point of the power source, respectively. $S_{xpi}, S_{xni} \in \{0,1\}$ with $x = A,B,C$, $i = 1,2$ are the switching functions of the inverter devices (0: switch closed, 1: switch opened) and $S_{xni} = 1 - S_{xpi}$ (because of the complementary operation of the upper and lower switches of each inverter leg). Therefore, the common-mode voltage of (2.37) can be rewritten as:

$$\begin{aligned} v_{cm} = \frac{1}{6}\big[&\big(S_{Ap1} + S_{Bp1} + S_{Cp1} + S_{Ap2} + S_{Bp2} + S_{Cp2}\big)v_{pG} \\ &+ (S_{An1} + S_{Bn1} + S_{Cn1} + S_{An2} + S_{Bn2} + S_{Cn2})v_{nG}\big] \end{aligned} \tag{2.39}$$

Let $N_{sw} = S_{Ap1} + S_{Bp1} + S_{Cp1} + S_{Ap2} + S_{Bp2} + S_{Cp2}$, thus

$$v_{cm} = \frac{1}{6}\big[N_{sw}v_{pG} + (6 - N_{sw})v_{nG}\big] \tag{2.40}$$

where N_{sw} is the number of upper inverter switches closed.

The squared RMS value of the common-mode voltage is:

$$v_{cm_{RMS}}^2 = \frac{1}{36T}\int_0^T \big[N_{sw}v_{pG} + (6 - N_{sw})v_{nG}\big]^2 dt \tag{2.41}$$

where T is the period of v_{pG} (equals the period of v_{nG}). Further expansion yields:

$$36v_{cm_{RMS}}^2 = N_{sw}^2\frac{1}{T}\int_0^T v_{pG}^2 dt + 2N_{sw}(6 - N_{sw})\frac{1}{T}\int_0^T v_{pG}v_{nG}dt + (6 - N_{sw})^2\frac{1}{T}\int_0^T v_{nG}^2 dt \tag{2.42}$$

The voltages of the DC link rails are given by:

$$\begin{aligned} v_{pG} &= S_{ap}v_{ra} + S_{bp}v_{rb} + S_{cp}v_{rc} \\ v_{nG} &= S_{an}v_{ra} + S_{bn}v_{rb} + S_{cn}v_{rc} \end{aligned} \tag{2.43}$$

where v_{ra}, v_{rb} and v_{rc} are the converter input phase voltages and S_{xp}, S_{xn} with $x = a,b,c$ are the switching functions of the rectifier. Accordingly v_{pG} and v_{nG} will always be segments of different input phase voltages and

$$\big|v_{pG}(t)\big| = |v_{nG}(t - t_o)| \ , t_o \in \mathbb{R} \tag{2.44}$$

Thus

$$\int_0^T v_{pG}^2 dt = \int_0^T v_{nG}^2 dt \tag{2.45}$$

Differentiating (2.42) with respect to N_{sw} and equating to zero, it can be found that $v_{cm_{RMS}}^2$ (and implicitly $v_{cm_{RMS}}$) achieves a minimum value at $N_{sw} = 3$, which means that in order to reduce the RMS common-mode voltage at the machine terminals, only three upper inverter switches should be closed at each switching period.

This can be further investigated by considering a virtual midpoint of the DC link as a reference point (see point 0 in Fig. 2.2). Then, (2.37) can be rewritten as:

$$v_{cm} = \frac{1}{6}(v_{A10} + v_{B10} + v_{C10} + v_{A20} + v_{B20} + v_{C20}) + v_{0G} = v_{cm0} + v_{0G} \tag{2.46}$$

where the contributions of the input and output stages to the overall common-mode voltage have been separated (v_{0G} and v_{cm0}, respectively). The voltage v_{0G} is the voltage between the reference point 0 and the grounded neutral point of the source. This voltage can be calculated as:

$$v_{0G} = \frac{1}{2}\left[\left(S_{ap} + S_{an}\right)v_{ra} + \left(S_{bp} + S_{bn}\right)v_{rb} + \left(S_{cp} + S_{cn}\right)v_{rc}\right] \tag{2.47}$$

It can be noted in (2.47) that v_{0G} depends on the modulation of the input stage, which is totally defined by the duty cycles of the rectifier stage. Thus, v_{0G} will have a predictable and bounded value. On the other hand, the voltage v_{cm0} can be rewritten as:

$$v_{cm0} = \frac{1}{6}\left[N_{sw}\frac{v_{DC}}{2} + (6 - N_{sw})\frac{v_{DC}}{2}\right] = \frac{1}{6}[N_{sw}v_{DC} - 3v_{DC}] \tag{2.48}$$

Therefore, it can be seen in (2.48) that by using $N_{sw} = 3$, the contribution of the output inverters to the common-mode voltage is eliminated [27].

The common-mode voltage produced by the 64 switching states combinations of the dual-inverter topology (v_{cm0}) can be calculated with (2.46) and are shown in Table 2.5.

Table 2.5. Active space vectors producing null common-mode voltage

V_{cm0}	Voltage vector combinations
$-V_{DC}/4$	V_{88}
$-V_{DC}/6$	$V_{85}, V_{83}, V_{81}, V_{58}, V_{38}, V_{18}$
$-V_{DC}/12$	$V_{84}, V_{86}, V_{82}, V_{55}, V_{35}, V_{33}, V_{51}, V_{31}$ $V_{15}, V_{13}, V_{11}, V_{48}, V_{68}, V_{28}, V_{53}$
0	$V_{14}, V_{25}, V_{36}, V_{52}, V_{87}, V_{54}, V_{34}, V_{56}, V_{32}, V_{16}$ $V_{12}, V_{45}, V_{43}, V_{41}, V_{65}, V_{63}, V_{23}, V_{21}, V_{78}, V_{61}$
$+V_{DC}/12$	$V_{17}, V_{57}, V_{37}, V_{44}, V_{46}, V_{64}, V_{24}, V_{42}$ $V_{62}, V_{26}, V_{22}, V_{75}, V_{73}, V_{66}, V_{71}$
$+V_{DC}/6$	$V_{47}, V_{74}, V_{76}, V_{67}, V_{72}, V_{27}$
$+V_{DC}/4$	V_{77}

Therefore reducing the common-mode voltage in an open-end winding machine drive is feasible if voltage vectors contained in the fourth row in Table 2.4 are used. However, it can be noted from Table 2.3 and Table 2.5 that the space vector combinations of the dual-inverter topology which eliminate the zero sequence voltage are not the same vectors which reduce the common-mode voltage. This should be considered when selecting the space vectors to modulate the output stages of the IMC in the proposed topology (Fig. 2.2), as will be discussed in chapter 3.

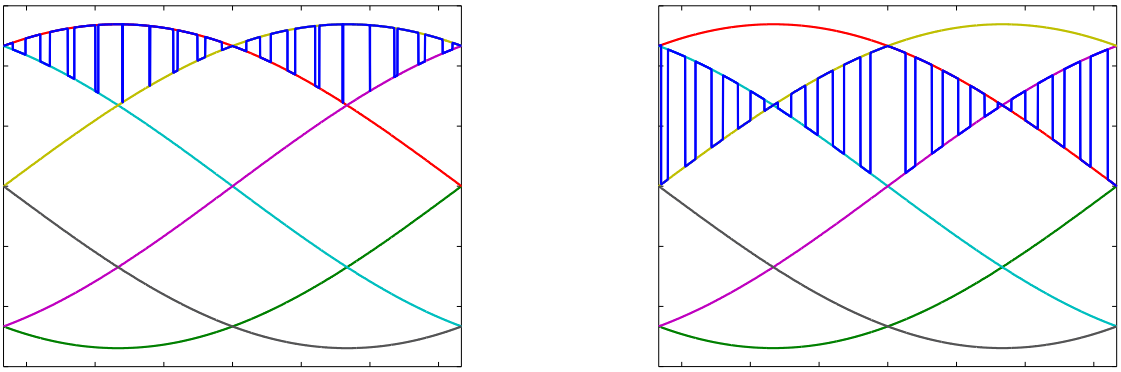
Chapter 3. Modulation strategies for the IMC

This chapter presents and analyzes different modulation strategies for the two-output IMC feeding an open-end winding induction machine. For the converter input stage, two Space Vector Modulation (SVM) strategies are shown: One produces a reduced DC voltage and the other maximizes the DC link voltage. For the converter output stages three PWM strategies are presented: A carrier-based PWM that produces a very low distorted input currents and two SVM strategies intended to reduce the zero sequence and/or the common-mode voltages.

3.1. Modulation for the input stage

The modulation strategy for the rectifier input stage of the power converter aims to obtain a positive DC link voltage during each sampling period and unity displacement factor at the input [65]. Moreover, the duty cycles used in the switching pattern should allow having sinusoidal currents at the converter input.

Two different SVM strategies can be used in the rectifier [66] and the possible DC link voltage waveforms are shown in Fig. 3.1. Usually, the input stage of an IMC is modulated in order to maximize the DC voltage by commutating between the largest and second largest positive line input voltage [66] (Fig. 3.1a). This strategy allows maximizing the converter voltage gain. However, if the converter output voltage requirement is low, the rectifier could be modulated to produce a reduced DC voltage commutating between the lowest and second lowest input line voltage [66] (Fig. 3.1b); this strategy allows the input and output stages of the power converter to commutate with lower voltage thus reducing the switching losses. The details of both SVM strategies are discussed below.



a) b)

Fig. 3.1. a) Maximum DC voltage. b) Reduced DC voltage

3.1.1 Modulation strategy for maximum DC voltage

A scheme for the input stage of the IMC is shown in Fig. 3.2, considering ideal bidirectional switches for the power devices. To maximize the DC link voltage, the sectors defined in Fig. 3.3 should be considered, where $\underline{i}_{ref}$ is the current reference vector. It can be noted in Fig. 3.3a that in each sector there is one positive phase voltage and two negative phase voltages, or vice versa. The operation consist on keeping closed the upper (or lower) switch corresponding to the highest absolute value of the input phase voltages and commutate the two lower (or upper) switches corresponding to the other input phase voltages; this results in a DC voltage composed by segments of the highest input line-to-line voltages in each sector (Fig. 3.1a).

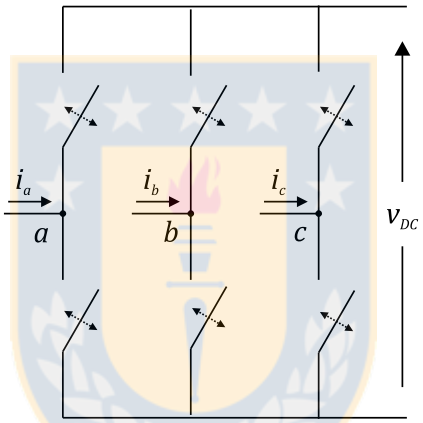


Fig. 3.2. Scheme of the IMC input stage

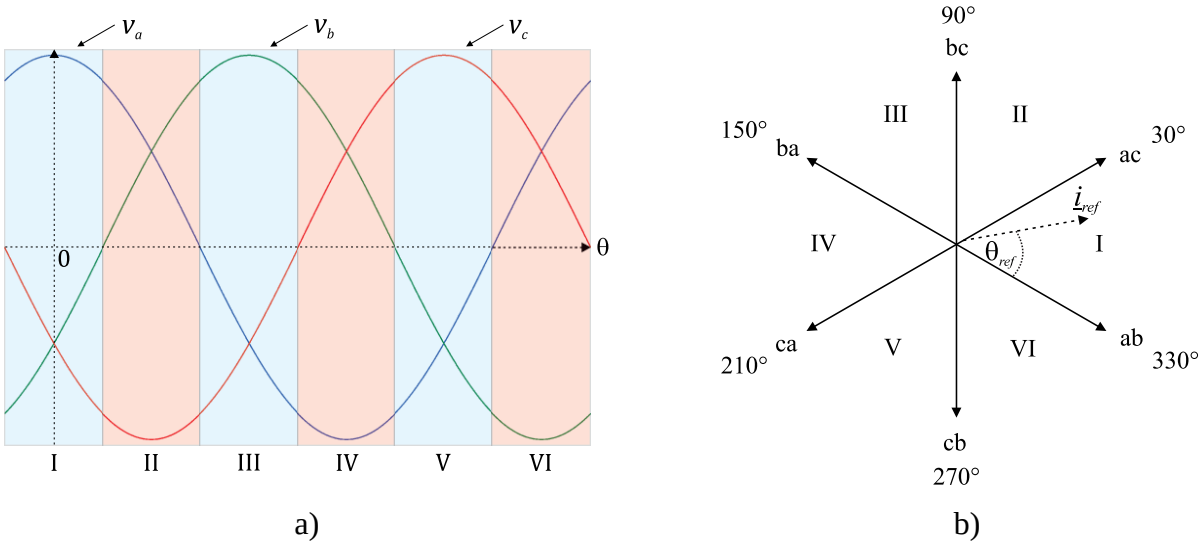


Fig. 3.3. a) Sectors defined by the input voltages and b) Locus of sectors and vectors for maximum DC voltage

Table 3.1 shows the input current in each sector, depending on the switch combination and the DC current i_{DC} [71]. The duty cycle subscript indicates the input line voltage reflected to the DC bus, with the first letter being the phase of the upper switch closed and the second letter the phase of the lower switch closed.

Table 3.1. Input currents for maximum DC voltage

Sector	Input current	Sector	Input current
I	$i_a = (d_{ab} + d_{ac})i_{DC}$ $i_b = -d_{ab}i_{DC}$ $i_c = -d_{ac}i_{DC}$	**IV**	$i_a = -(d_{ba} + d_{ca})i_{DC}$ $i_b = d_{ba}i_{DC}$ $i_c = d_{ca}i_{DC}$
II	$i_a = d_{ac}i_{DC}$ $i_b = d_{bc}i_{DC}$ $i_c = -(d_{ac} + d_{bc})i_{DC}$	**V**	$i_a = -d_{ca}i_{DC}$ $i_b = -d_{cb}i_{DC}$ $i_c = (d_{ca} + d_{cb})i_{DC}$
III	$i_a = -d_{ba}i_{DC}$ $i_b = (d_{ba} + d_{bc})i_{DC}$ $i_c = -d_{bc}i_{DC}$	**VI**	$i_a = d_{ab}i_{DC}$ $i_b = -(d_{ab} + d_{cb})i_{DC}$ $i_c = d_{cb}i_{DC}$

From Table 3.1, the Sector I duty cycles are:

$$d_{ab} + d_{ac} = \frac{i_a}{i_{DC}}; \quad d_{ab} = -\frac{i_b}{i_{DC}}; \quad d_{ac} = -\frac{i_c}{i_{DC}} \tag{3.1}$$

Because the zero vectors are not used, the duty cycles need to satisfy the following relationship:

$$d_{ab} + d_{ac} = 1 \tag{3.2}$$

which implies, from eq. (3.1), that $i_{DC} = i_a$. Then the duty cycles are given by

$$d_{ab} = -\frac{i_b}{i_a}; \quad d_{ac} = -\frac{i_c}{i_a} \tag{3.3}$$

For unity displacement factor, the reference input currents are in phase with the phase input voltages:

$$v_a = V\cos(\theta) \quad \Longrightarrow \quad i_a = I\cos(\theta) \tag{3.4}$$

$$v_b = V\cos(\theta - 120°) \quad \Longrightarrow \quad i_b = I\cos(\theta - 120°) \tag{3.5}$$

$$v_c = V\cos(\theta + 120°) \quad \Longrightarrow \quad i_c = I\cos(\theta + 120°) \tag{3.6}$$

Therefore the duty cycles of eq. (3.3) can be rewritten as:

$$d_{ab} = -\frac{i_b}{i_a} = -\frac{\cos(\theta - 120°)}{\cos(\theta)} \Longrightarrow d_{ab} = \frac{\sin(30° - \theta)}{\cos(\theta)} \tag{3.7}$$

$$d_{ac} = -\frac{i_c}{i_a} = -\frac{\cos(\theta + 120°)}{\cos(\theta)} \Longrightarrow d_{ac} = \frac{\sin(150° - \theta)}{\cos(\theta)} \tag{3.8}$$

From (3.4)-(3.6) and Table 3.1, the duty cycles for each sector can be calculated as shown in Table 3.2 [71]. The θ_{ref} angle corresponds to the angle of the reference vector current referred to the sector where $\underline{i}_{ref}$ is located; this angle is a function of θ and is also shown in Table 3.2.

Table 3.2. Duty cycles for maximum DC voltage

Sector	d_γ^R	d_δ^R	θ_{ref}
I	$d_{ab} = -\frac{i_b}{i_a} = \frac{\sin(30° - \theta)}{\cos(\theta)}$	$d_{ac} = -\frac{i_c}{i_a} = \frac{\sin(150° - \theta)}{\cos(\theta)}$	$\theta + 30°$
II	$d_{ac} = -\frac{i_a}{i_c} = \frac{\sin(90° - \theta)}{\sin(\theta + 30°)}$	$d_{bc} = -\frac{i_b}{i_c} = \frac{\sin(\theta - 30°)}{\sin(\theta + 30°)}$	$\theta - 30°$
III	$d_{bc} = -\frac{i_c}{i_b} = \frac{\sin(150° - \theta)}{\sin(\theta - 30°)}$	$d_{ba} = -\frac{i_a}{i_b} = \frac{\sin(\theta - 90°)}{\sin(\theta - 30°)}$	$\theta - 90°$
IV	$d_{ba} = -\frac{i_b}{i_a} = \frac{\sin(\theta - 30°)}{\sin(\theta - 90°)}$	$d_{ca} = -\frac{i_c}{i_a} = \frac{\sin(\theta - 150°)}{\sin(\theta - 90°)}$	$\theta - 150°$
V	$d_{ca} = -\frac{i_a}{i_c} = \frac{\sin(\theta - 90°)}{\sin(\theta - 150°)}$	$d_{cb} = -\frac{i_b}{i_c} = \frac{\sin(30° - \theta)}{\sin(\theta - 150°)}$	$\theta - 210°$
VI	$d_{cb} = -\frac{i_c}{i_b} = \frac{\sin(\theta - 150°)}{\sin(30° - \theta)}$	$d_{ab} = -\frac{i_a}{i_b} = \frac{\sin(90° - \theta)}{\sin(30° - \theta)}$	$\theta - 270°$

Considering the sector angle of the reference vector θ_{ref}, the duty cycles d_γ^R and d_δ^R can be calculated as [65]:

$$d_\gamma^R = \frac{\sin(60° - \theta_{ref})}{\sin(60° - \theta_{ref}) + \sin(\theta_{ref})} \quad , \quad d_\delta^R = \frac{\sin(\theta_{ref})}{\sin(60° - \theta_{ref}) + \sin(\theta_{ref})} \tag{3.9}$$

and defining

$$d_\gamma = \sin(60° - \theta_{ref}) \quad , \quad d_\delta = \sin(\theta_{ref}) \tag{3.10}$$

eq. (3.9) can be rewritten as:

$$d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta} \quad , \quad d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \tag{3.11}$$

Finally, as shown in [71], with this modulation strategy the maximum theoretical average DC voltage is limited to $\frac{\sqrt{3}}{2}\hat{V}_{i,l-l}$, where $\hat{V}_{i,l-l}$ is the peak input line-to-line voltage of the converter.

3.1.2 Modulation strategy for reduced DC voltage

If a reduced DC link voltage is required, the sectors defined in Fig. 3.4 should be considered. As can be seen in Fig. 3.4a, in each sector there is a positive voltage, a negative voltage and a voltage changing from positive to negative, or vice versa. In this case, opposite the modulation for maximum DC voltage, there are commutations in both the upper and lower switches of the converter in each sector. The result is a DC voltage composed by segments of the lower input line-to-line voltages (Fig. 3.1b).

The input currents as a function of the duty cycles and the DC current, for each sector, are shown in Table 3.3 [71].

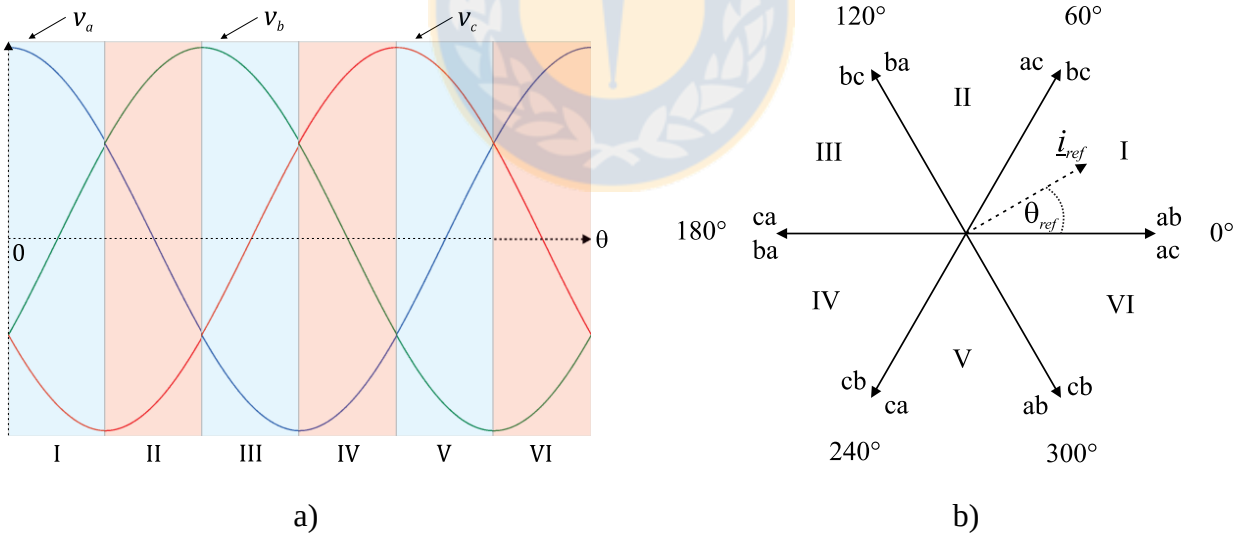


Fig. 3.4. a) Sectors defined by the input voltages and b) Locus of sectors and vectors for reduced DC voltage

Table 3.3. Input currents for reduced DC voltage

Sector	Input current	Sector	Input current
I	$i_a = d_{ab} i_{DC}$ $i_b = (d_{bc} - d_{ab}) i_{DC}$ $i_c = -d_{bc} i_{DC}$	**IV**	$i_a = -d_{ba} i_{DC}$ $i_b = (d_{ba} - d_{cb}) i_{DC}$ $i_c = d_{cb} i_{DC}$
II	$i_a = (d_{ac} - d_{ba}) i_{DC}$ $i_b = d_{ba} i_{DC}$ $i_c = -d_{ac} i_{DC}$	**V**	$i_a = (d_{ab} - d_{ca}) i_{DC}$ $i_b = -d_{ab} i_{DC}$ $i_c = d_{ca} i_{DC}$
III	$i_a = -d_{ca} i_{DC}$ $i_b = d_{bc} i_{DC}$ $i_c = (d_{ca} - d_{bc}) i_{DC}$	**VI**	$i_a = d_{ac} i_{DC}$ $i_b = -d_{cb} i_{DC}$ $i_c = (d_{cb} - d_{ac}) i_{DC}$

Considering Table 3.3, the duty cycles for Sector I are:

$$d_{bc} - d_{ab} = \frac{i_b}{i_{DC}}; \quad d_{ab} = \frac{i_a}{i_{DC}}; \quad d_{bc} = -\frac{i_c}{i_{DC}} \tag{3.12}$$

Moreover, as the zero vector vectors are not used:

$$d_{ab} + d_{bc} = 1 \Longrightarrow d_{bc} = 1 - d_{ab} \Longrightarrow i_b = (1 - 2d_{ab}) i_{DC} \tag{3.13}$$

and with (3.12) and (3.13), the DC current can be obtained:

$$i_b = (1 - 2d_{ab}) i_{DC} \Longrightarrow i_b = i_{DC} - 2d_{ab} i_{DC} \tag{3.14}$$

$$i_{DC} = 2i_a + i_b = i_a - i_c = i_{ac} \tag{3.15}$$

Then, the duty cycles for Sector I are:

$$d_{ab} = \frac{i_a}{i_{ac}}; \quad d_{bc} = -\frac{i_c}{i_{ac}} \tag{3.16}$$

To obtain unity displacement factor at the converter input, (3.16) can be rewritten as:

$$d_{ab} = \frac{i_a}{i_{ac}} \Longrightarrow d_{ab} = \frac{\cos(\theta)}{\cos(\theta) - \cos(\theta + 120°)} \tag{3.17}$$

$$d_{bc} = -\frac{i_c}{i_{ac}} \Longrightarrow d_{bc} = -\frac{\cos(\theta + 120°)}{\cos(\theta) - \cos(\theta + 120°)} \tag{3.18}$$

From (3.4)-(3.6) and Table 3.3, the duty cycles for all sectors can be calculated and are summarized in Table 3.4, including the reference vector angle θ_{ref} [71].

Table 3.4. Duty cycles for reduced DC voltage

Sector	d_γ^R	d_δ^R	θ_{ref}
I	$d_{ab} = \frac{i_a}{i_{ac}} = \frac{\cos(\theta)}{\sqrt{3}\cos(\theta - 30°)}$	$d_{bc} = -\frac{i_c}{i_{ac}} = -\frac{\cos(\theta + 120°)}{\sqrt{3}\cos(\theta - 30°)}$	θ
II	$d_{ac} = -\frac{i_c}{i_{bc}} = -\frac{\cos(\theta + 120°)}{\sqrt{3}\cos(\theta - 90°)}$	$d_{ba} = \frac{i_b}{i_{bc}} = \frac{\cos(\theta - 120°)}{\sqrt{3}\cos(\theta - 30°)}$	$\theta - 60°$
III	$d_{bc} = \frac{i_b}{i_{ba}} = \frac{\cos(\theta - 120°)}{\sqrt{3}\cos(\theta - 150°)}$	$d_{ca} = -\frac{i_a}{i_{ba}} = -\frac{\cos(\theta)}{\sqrt{3}\cos(\theta - 30°)}$	$\theta - 120°$
IV	$d_{ba} = -\frac{i_a}{i_{ca}} = -\frac{\cos(\theta)}{\sqrt{3}\cos(\theta - 210°)}$	$d_{cb} = \frac{i_c}{i_{ca}} = \frac{\cos(\theta + 120°)}{\sqrt{3}\cos(\theta - 210°)}$	$\theta - 180°$
V	$d_{ca} = \frac{i_c}{i_{cb}} = \frac{\cos(\theta + 120°)}{\sqrt{3}\cos(\theta + 90°)}$	$d_{ab} = -\frac{i_b}{i_{cb}} = -\frac{\cos(\theta - 120°)}{\sqrt{3}\cos(\theta + 90°)}$	$\theta - 240°$
VI	$d_{cb} = -\frac{i_b}{i_{ab}} = -\frac{\cos(\theta - 120°)}{\sqrt{3}\cos(\theta + 30°)}$	$d_{ac} = \frac{i_a}{i_{ab}} = \frac{\cos(\theta)}{\sqrt{3}\cos(\theta + 30°)}$	$\theta - 300°$

Considering the reference vector angle θ_{ref}, the duty cycles d_γ^R and d_δ^R can be expressed as:

$$d_\gamma^R = \frac{\cos(\theta_{ref})}{\cos(\theta_{ref}) + \cos(60° - \theta_{ref})} \quad , \quad d_\delta^R = \frac{\cos(60° - \theta_{ref})}{\cos(\theta_{ref}) + \cos(60° - \theta_{ref})} \tag{3.19}$$

and defining

$$d_\gamma = \cos(\theta_{ref}) \quad , \quad d_\delta = \cos(60° - \theta_{ref}) \tag{3.20}$$

the duty cycles d_γ^R and d_δ^R are given by (3.11).

As derived in [71], with this modulation strategy the maximum theoretical average DC voltage is limited to $\frac{1}{2}\hat{V}_{i,l-l}$, where $\hat{V}_{i,l-l}$ is the peak input line-to-line voltage of the converter.

3.2. Modulation strategies for the output stages of the IMC

The output stages of the IMC should produce the voltage and frequency required by the load. To achieve this objective, three modulation strategies for the dual-inverter are proposed and analyzed in this section.

3.2.1 Carrier-based modulation strategy

The carrier-based PWM strategy is a standard modulation technique for power inverters [67]. A triangular (carrier) signal v_{tri} is compared with a sinusoidal (reference) signal v_{ref}, as shown in Fig. 3.5, and the following control logic is used to generate the IGBTs gate pulses:

$$v_{ref} \geq v_{tri} \Longrightarrow S_{xpk} = 1$$

$$v_{ref} < v_{tri} \Longrightarrow S_{xpk} = 0$$

where S_{xpk} with $x = a, b, c$, $k = 1,2$ is an upper switch of the dual-inverter.

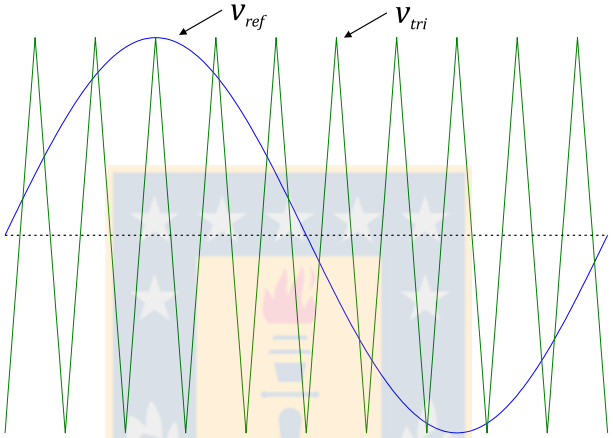


Fig. 3.5. Signals used in a carrier-based modulation strategy

The duty cycles for each leg of the IMC output stages are [72]:

Inverter 1 duty cycles	Inverter 2 duty cycles	
$d_{a1} = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k\right)+1\right)$	$d_{a2} = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k+\pi\right)+1\right)$	(3.21)
$d_{b1} = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k-\frac{2\pi}{3}\right)+1\right)$	$d_{b2} = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k-\frac{2\pi}{3}+\pi\right)+1\right)$	(3.22)
$d_{c1} = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k+\frac{2\pi}{3}\right)+1\right)$	$d_{c2} = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k+\frac{2\pi}{3}+\pi\right)+1\right)$	(3.23)

where $m_f = f_s/f_o$ is the frequency index (f_o: output frequency, f_s: switching frequency) and $0 \leq k \leq m_f$. The fluctuations of the average DC link voltage in every switching period should be compensated by means of the modulation index of output inverters. This results in a variable modulation index given by $m(t) = m_o(d_\gamma + d_\delta)$, where m_o is the final modulation index ($0 \leq m_o \leq 1$).

It can be noted from (3.21)-(3.23) that the phase with the lower duty cycle in inverter 1 will be the phase with the higher duty cycle in inverter 2, and vice versa. The phase with the middle duty cycle is the same for both output inverters. Fig. 3.6 shows a representation of the duty cycles. For implementation purposes, d_a, d_b and d_c are transformed into equivalent $\alpha - \beta - 0$ duty cycles. From Fig. 3.6 it can be obtained that the $\alpha - \beta - 0$ duty cycles are given by:

$$d_\alpha = d_{max} - d_{mid}\ ,\ d_\beta = d_{mid} - d_{min} \tag{3.24}$$

$$d_0 = 1 - d_{max}\ ,\ d_7 = d_{min} \tag{3.25}$$

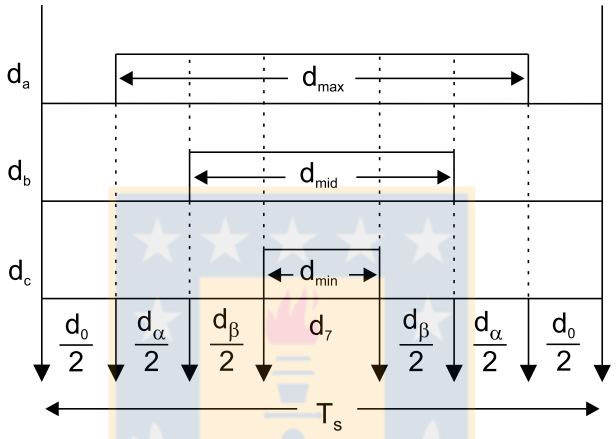


Fig. 3.6. A single inverter stage duty cycles

Finally, to obtain a correct balance of the input currents and the output voltages in a switching period, the modulation pattern should produce all combinations of the rectification and the inversion switching states [65], resulting in the following duty cycles for the active vectors:

$$d_{\alpha\gamma} = d_\alpha d_\gamma^R\ ,\ d_{\beta\gamma} = d_\beta d_\gamma^R\ ,\ d_{\alpha\delta} = d_\alpha d_\delta^R\ ,\ d_{\beta\delta} = d_\beta d_\delta^R \tag{3.26}$$

The duty cycle corresponding to the switching state $[S_{Ap}\ S_{Bp}\ S_{Cp}] = [0\ 0\ 0]$ is:

$$d_{00} = d_{0,tot} - d_{min} \tag{3.27}$$

where $d_{0,tot}$ is the total duty cycle for the zero states ($[0\ 0\ 0], [1\ 1\ 1]$) and is given by:

$$d_{0,tot} = 1 - (d_\alpha + d_\beta)(d_\gamma^R + d_\delta^R) \tag{3.28}$$

and the combined zero vectors duty cycles are:

$$d_{0\gamma} = d_{00} d_\gamma^R\ ,\ d_{0\delta} = d_{00} d_\delta^R \tag{3.29}$$

The output stages duty cycles, which are different for each inverter, are represented in Fig. 3.7.

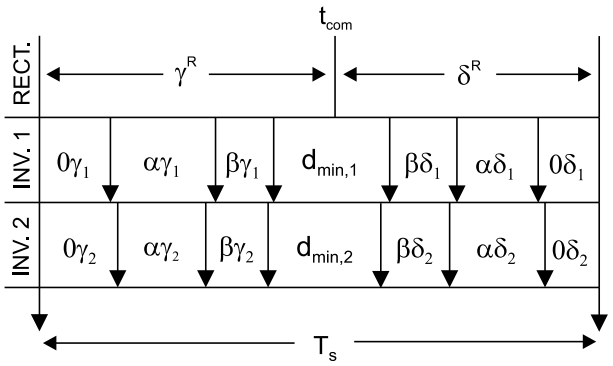


Fig. 3.7. Inverters duty cycles

The carrier-based modulation strategy discussed above is one of the simplest methods to modulate a voltage source inverter and has been shown that can be easily adapted to modulate the output stages of the IMC.

3.2.2 SVM strategy for zero sequence voltage reduction

As mentioned in chapter 2, in an open-end winding induction machine fed by a dual-inverter with a single DC source, a zero sequence current could circulate in the machine windings then producing the problems associated to it. However, the zero sequence voltage applied to the machine can be eliminated by using certain voltage space vectors as shown in Table 2.3. Moreover, it has been mentioned that there are two equivalent sets of active vectors producing $v_{zs} = 0$ that can be used along with eight null vectors available in the dual-inverter. The locus of the vectors producing null v_{zs} is shown in Fig. 3.8.

As can be seen in Fig. 3.8, the hexagon is divided into six sectors and among the eight null vectors available, only six are finally used (three null vectors per set) [28]. Moreover the null vectors should be mapped depending on the sector information [28] in order to reduce the commutations in a period. The mapping is shown in Table 3.5.

Table 3.5. Mapping of zero vectors

Sector	**I**	**II**	**III**	**IV**	**V**	**VI**
Set 1 zero vectors	V_{55}	V_{33}	V_{11}	V_{55}	V_{33}	V_{11}
Set 2 zero vectors	V_{44}	V_{22}	V_{66}	V_{44}	V_{22}	V_{66}

From Table 2.4 and 3.5 it can be noted that in each sector one of the inverters keeps clamped in a specific state and the other inverter commutates between three different switching states. This allows reducing the switching losses of the converter output stages.

The zero vectors V_{77} and V_{88} are not considered for this modulation scheme since none of the active vectors (Table 2.4) use the states $V_7 = [1\ 1\ 1]$ or $V_8 = [0\ 0\ 0]$ for the individual inverters. Hence the application of V_{77} or V_{88} in the output stages will result in more commutations per period and thus in higher switching losses than the strategy proposed with the mapping of Table 3.5. However, these zero states are available if vectors redundancy is required.

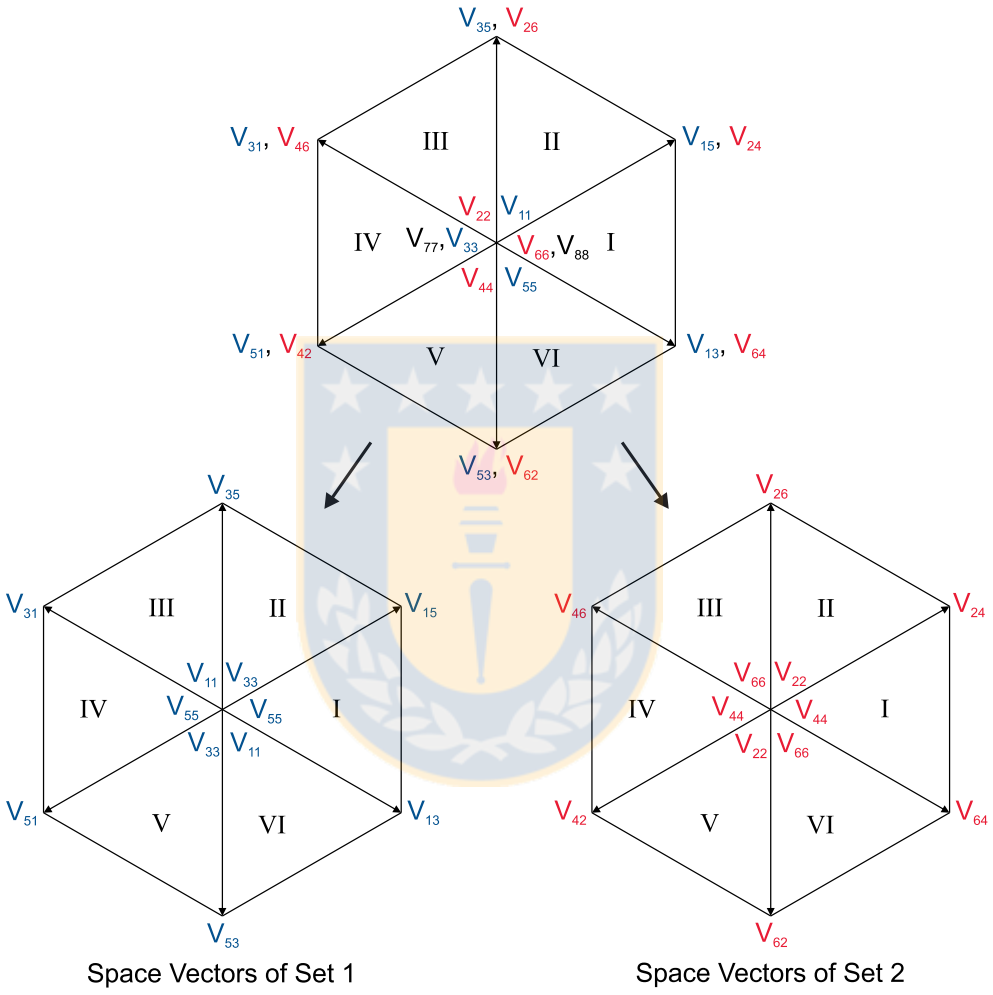


Fig. 3.8. Locus of vectors producing null zero sequence voltage

To apply the switching states of the dual-inverter, the following duty cycles are considered for the active vectors [65]:

$$d_\alpha = m(t)\sin\left(\pi/3 - \theta_{ref,o}\right) \quad , \quad d_\beta = m(t)\sin\left(\theta_{ref,o}\right) \tag{3.30}$$

where $\theta_{ref,o}$ is the angle of the output reference voltage vector, $m(t) = m_o\left(d_\gamma + d_\delta\right)$ is a variable modulation index to compensate the variable DC link voltage of the IMC and m_o is a final modulation index.

The duty cycle of the zero vectors is given by:

$$d_0 = 1 - d_\alpha - d_\beta \tag{3.31}$$

As in the carrier-based modulation strategy, the duty cycles of the rectifier and the inverters should be combined, thus the active vector duty cycles are given in (3.14) and the combined zero vectors duty cycles are:

$$d_{0\gamma} = d_0 d_\gamma^R \ , \ d_{0\delta} = d_0 d_\delta^R \tag{3.32}$$

Finally, the switching sequence, which is the same for both output stages, is shown in Fig. 3.9, commutating the input stage with zero DC current [65].

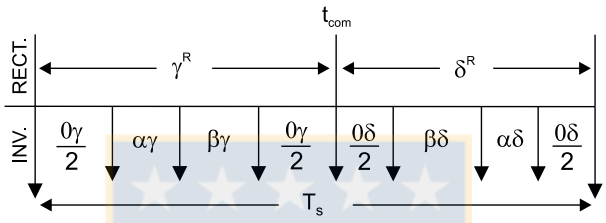


Fig. 3.9. Standard switching sequence for IMCs

The space vector modulation presented allows reducing the output zero sequence voltage then reducing the undesirable effects of the zero sequence currents. Moreover there is voltage vectors redundancy thus allowing choosing between two equivalent sets of vectors producing the same machine phase voltage.

3.2.3 SVM strategy for common-mode voltage reduction

In chapter 2 it has been shown that an open-end winding machine drive offers the possibility of reducing the common-mode voltage by using certain voltage space vector combinations of the dual-inverter [27], as shown in Table 2.5. The locus of the vectors that theoretically eliminate the contribution of the IMC output stages to the overall common-mode voltage of the drive is shown in Fig. 3.10.

As can be noted in the locus, the vectors that reduce the common-mode voltage are the largest and some of the lowest, then depending on the output voltage requirement the modulation for the dual-inverter could use the vectors of Fig. 3.10a or Fig. 3.10b. Moreover, for the lowest vectors there is switching states redundancy, opposite the situation for the largest ones where all the voltage vectors can be produced by a unique switching state combination of the IMC output stages.

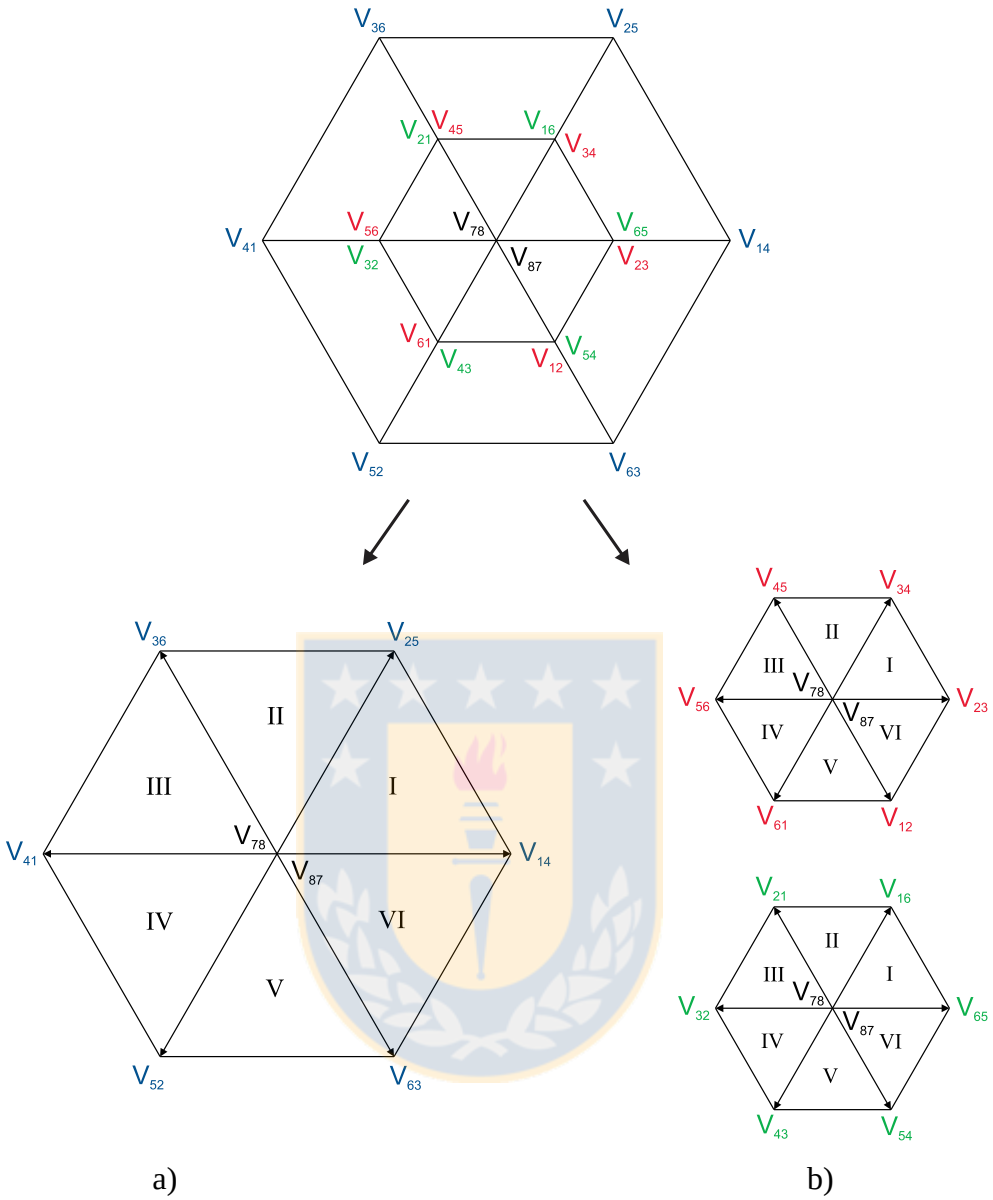


Fig. 3.10. Locus of vectors for reduced common-mode voltage

However, despite the aforementioned advantage of the lowest vectors, for the modulation strategy proposed, only the largest vectors will be used attending to maximize the output voltage and because the using of all the vectors available will complicate the modulation algorithm and the benefits in terms of current/voltage THD of applying the lowest space vectors are not significant.

On the other hand, it can be appreciated that the zero vectors producing null common-mode voltage (V_{78} and V_{87}) do generate output phase voltage, then in this case the input rectifier of the IMC will not commutate with zero current, thus increasing the switching losses.

As mentioned in chapter 2, the vectors that reduce the common-mode voltage will produce zero sequence voltage as can be noted in Table 2.3 and 2.5. Therefore, compensation must be performed in order to avoid the circulation of zero sequence currents in the machine.

The compensation consists on eliminating the average zero sequence voltage within a sampling interval by forcing the zero sequence volt-seconds to zero [24]. This can be done by applying the null voltage vectors with unequal times [24] then modifying the standard switching pattern for IMCs shown in Fig. 3.9 and commutating the output stages of the IMC with the switching pattern of Fig. 3.11.

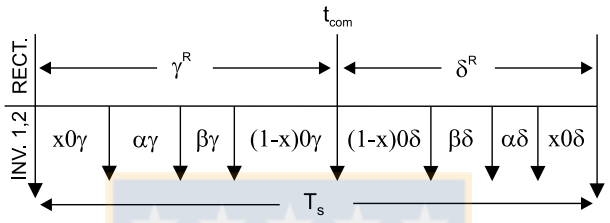


Fig. 3.11. Modified switching sequence for the IMC with two outputs

As it is known which space vector will be applied in every switching period, it can be known what the zero sequence voltage will be in every switching period as well. Thus, taking into account that the same space vectors sequence applied in γ^R interval is applied in the δ^R interval but in reverse order, then the value of x, which causes the cancellation of the zero sequence volt-seconds, is calculated at every sampling period to satisfy [24]:

$$v_{zs1}x\left(d_{0\gamma}+d_{0\delta}\right)+v_{zs2}\left(d_{\alpha\gamma}+d_{\alpha\delta}\right)+v_{zs3}\left(d_{\beta\gamma}+d_{\beta\delta}\right)+v_{zs4}(1-x)\left(d_{0\gamma}+d_{0\delta}\right)=0 \quad (3.33)$$

where v_{zsk} with $k=1,2,3,4$, is the zero sequence voltage value (calculated with eq. (2.32)) at intervals $xd_{0\gamma}$, $d_{\alpha\gamma}$, $d_{\beta\gamma}$ and $(1-x)d_{0\gamma}$, respectively.

Considering the voltage vectors of Fig. 3.10a and Table 2.2 it can be obtained that in any sector the zero sequence voltage at the different intervals are:

$$v_{zs1}=-V_{DC}/2 \quad , \quad v_{zs2}=-V_{DC}/6 \quad , \quad v_{zs3}=+V_{DC}/6 \quad , \quad v_{zs4}=+V_{DC}/2 \quad (3.34)$$

Replacing the voltages of (3.34) in (3.33), a solution for x can be found:

$$x=\frac{1}{2}+\frac{d_{\beta\gamma}+d_{\beta\delta}-d_{\alpha\gamma}-d_{\alpha\delta}}{6\left(d_{0\gamma}+d_{0\delta}\right)} \quad (3.35)$$

This coefficient must be calculated at every switching period of the IMC to allow a correct reduction of the output zero sequence volt-seconds.

The modulation strategy presented reduces the common-mode voltage produced by the output VSIs of the power converter and compensate the occurrence of zero sequence voltage. However, as the input rectifier of the IMC will commutate with current circulation, higher switching losses are expected compared to the SVM strategy that reduced the zero sequence voltage.

Chapter 4. Experimental System

This chapter describes the hardware used in the implementation of the experimental setup. The power system is based on a two-output Indirect Matrix Converter rated at 7.5 kW. This converter supplies energy to a 7.5 kW open-end winding induction machine. The control platform is based on a TMS3206713 Digital Signal Processor (DSP) and a Field Programmable Gate Array (FPGA). In this platform tasks such as data acquisition, modulation and control algorithms, and PWM signal generation are carried out. The details of both the power and control systems are given below.

4.1. Introduction

In the experimental system built to test the modulation strategies discussed in chapter 3, the main components are a 7.5 kW six pole induction machine and a two-output Indirect Matrix Converter. The measurement and control tasks are based in two main elements: an external board DSK C6713 which major component is the processor DSP TMS320C6713 and an interface board based on the FPGA A500K050 directly connected to the DSK board. In the interface board, the following tasks are implemented: Analog-to-Digital (A/D) conversion of the measured signals, programmable current/voltage protections, signal conditioning, PWM generation for the power converter and encoder lecture of the machine.

For load application to the induction machine, a separately excited DC generator supplying a variable resistor is used. The DC generator is directly coupled to the AC motor shaft.

To measure the rotor position, an incremental encoder of 10000 pulses per revolution is used along with a board designed to send the necessary signals for position measuring to the interface board.

In general, the major hardware components of the experimental setup can be summarized as:

- Dual-output indirect matrix converter.
- Induction machine.
- Direct current generator (load).
- DSK C6713 board.
- Interface board.
- Host Port Interface (HPI) board.

- Voltage measurement board.
- Current measurement board.
- Encoder and encoder reading board.
- Three-phase auto transformer.
- Twelve channel digital oscilloscope.

A brief description of every component of the experimental system is given below.

4.2. Dual-output indirect matrix converter

The two-output indirect matrix converter used in this thesis project is shown in Fig. 4.1. This power converter is a laboratory prototype, designed and built at the University of Nottingham Power Electronics, Machines and Control (PEMC) lab facilities. The converter has a rectifier stage and two inverter stages. Its rated power is 7.5 kW and includes seven Hall effect current sensors for the six output terminals and the DC link current. Moreover, the IMC has a clamping circuit to avoid over voltages in the DC link. The clamping circuit consists of eight Schottky diodes, two capacitors and an analogue protection circuit. The current measurements and a signal provided by the clamping protection circuit are available in a DB9 connector.

To operate the input rectifier by means of voltage or current commutation, the IMC has three circuits to measure the sign of all the input line voltages and a circuit to measure the sign of the DC link current.

The input filter of the converter consists of three capacitors of 2 μF connected in delta and three inductors of 0.5 mH. The switching frequency used is 10 kHz and the commutation time for the switches of the rectifier and the inverters is 2 μs.

The rectifier stage is built with discrete bidirectional switches corresponding to IGBTs modules SEMIKRON SK60GM123, see Fig. 4.2. Each inverter stage is built using an IGBTs module SEMIKRON SK35GD126 (full three-phase bridge inverter), shown in Fig. 4.3.

Fig. 4.4 shows a schematic diagram of the converter structure.

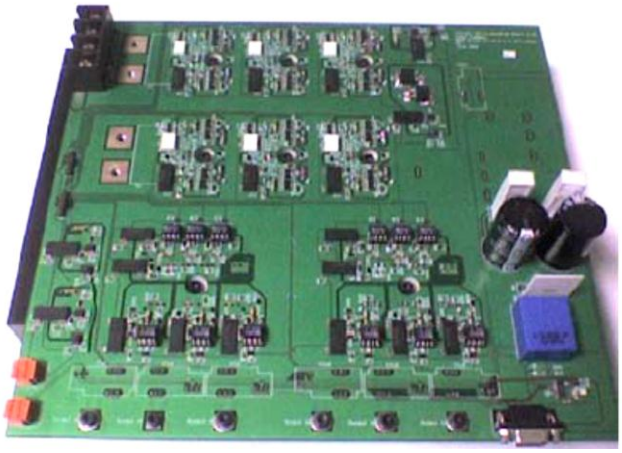


Fig. 4.1. Two-output indirect matrix converter

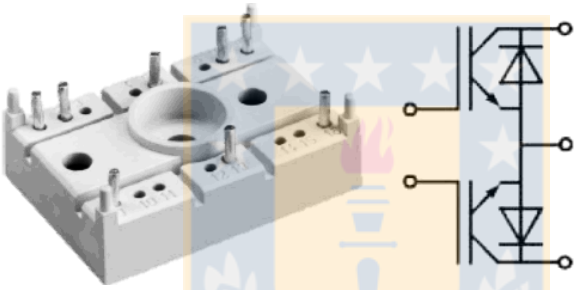


Fig. 4.2. Module SEMIKRON SK60GM123

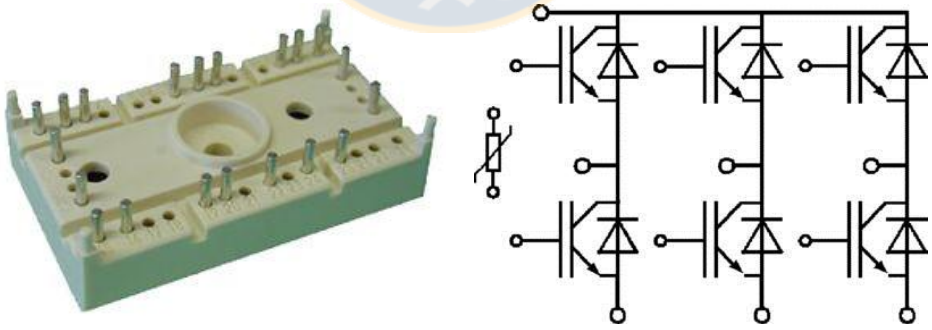


Fig. 4.3. Module SEMIKRON SK35GD126

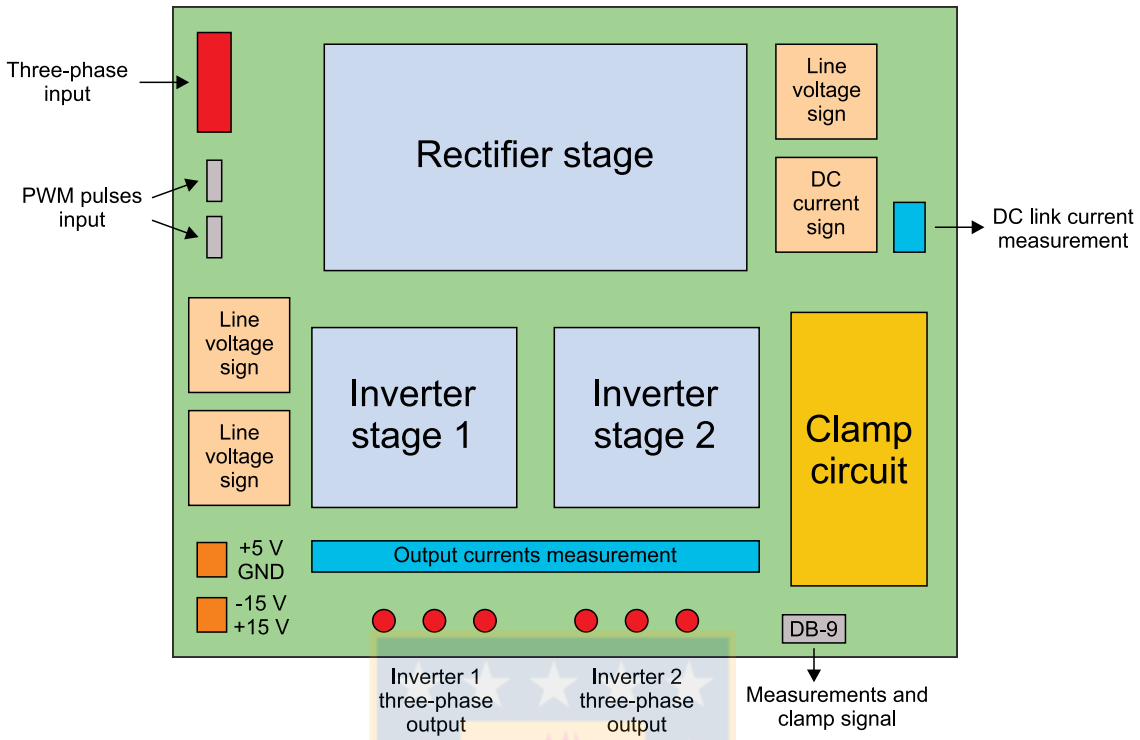


Fig. 4.4. Diagram of the two-output IMC structure

4.3. DSK C6713 board

The DSK C6713 board is a development platform built by *Texas Instrument* together with *Spectrum Digital*. Some of the main characteristics are:

- It is based on the DSP TMS320C6713.
- Operates with a clock frequency programmable up to 225 MHz.
- Up to 1800 MIPS (Millions of Instructions per Second).
- Up to 1350 MFLOPS (Millions of Floating Point Operations per Second).
- Expansion plugs for peripherals and memory.
- HPI Port.

Fig. 4.5 shows the diagram of the internal structure of the DSK C6713 board. The board as such is shown in Fig. 4.6.

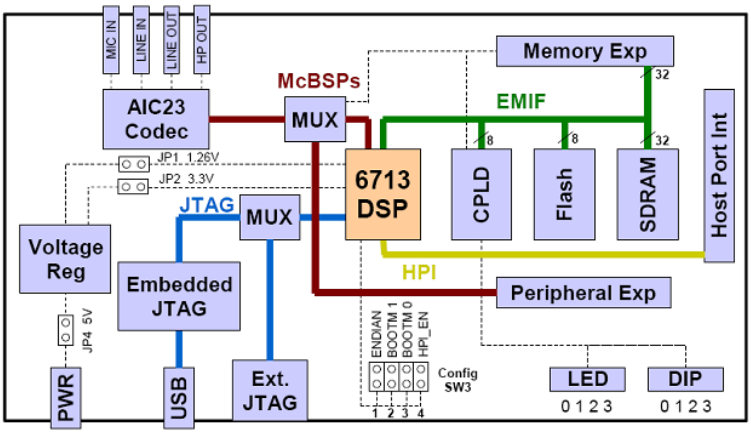


Fig. 4.5. Diagram of the DSK C6713 board

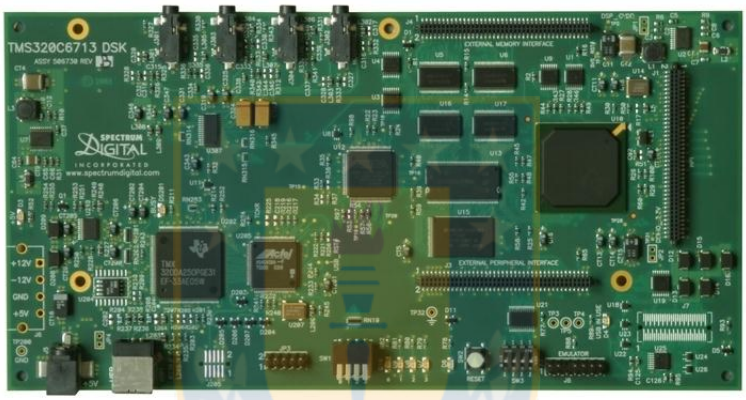


Fig. 4.6. DSK C6713 board

4.4. Host Port Interface (HPI) board

This board, built by *Educational DSP*, is connected to the HPI port of the DSK C6713 board allowing the communication between the DSK board and a computer by means of a USB port. The HPI board allows performing several tasks such as:

- Loading a program.
- Initialization and reset of the DSK board.
- Memory reading and writing.

Fig. 4.7 shows a diagram of the HPI structure while Fig. 4.8 shows the HPI board connected to a DSK C6713 board where the main components are indicated.

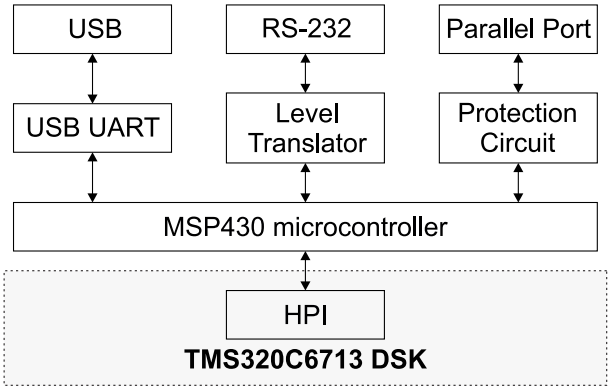


Fig. 4.7. Diagram of the HPI board structure

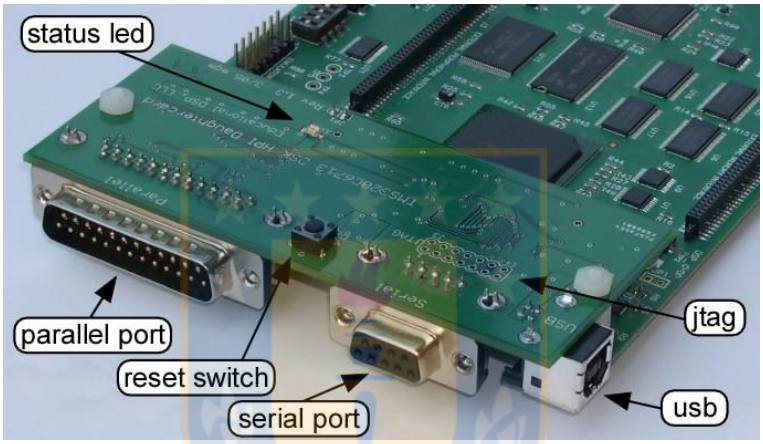


Fig. 4.8. HPI board

4.5. Interface board

The interface board, shown in Fig. 4.9 and developed by the Power Electronics, Machines and Control (PEMC) group of the University of Nottingham, is based on the FPGA Actel A500K050 and performs the tasks of A/D and D/A conversion, over current/voltage protection, encoder reading and PWM generation for the power converter. Moreover it has LEDs to display the system status.

This board is connected to DSK board by means of memory and peripherals expansion plugs. The main features of the interface board are:

- 10 channels for 12 bits A/D conversion.
- 4 channels for 12 bits D/A conversion.
- Programmable protections.
- Two encoder reading inputs.

- 10 MHz clock.
- Inputs for system reset and initialization.

Fig. 4.10 shows a diagram of the internal structure of the interface board.

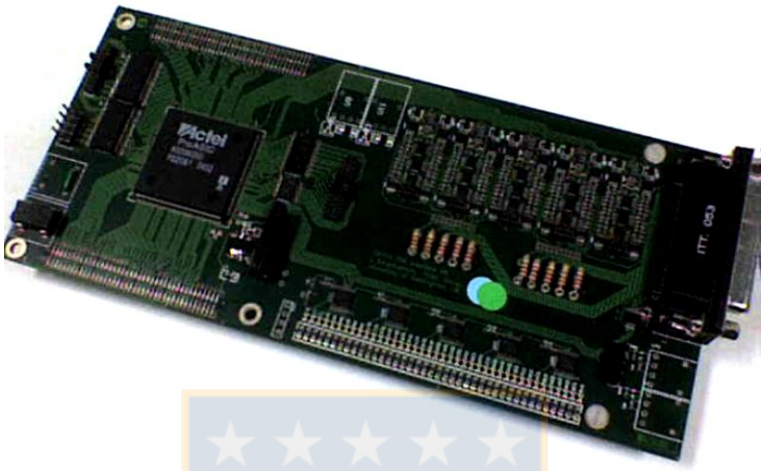


Fig. 4.9. FPGA-based interface board

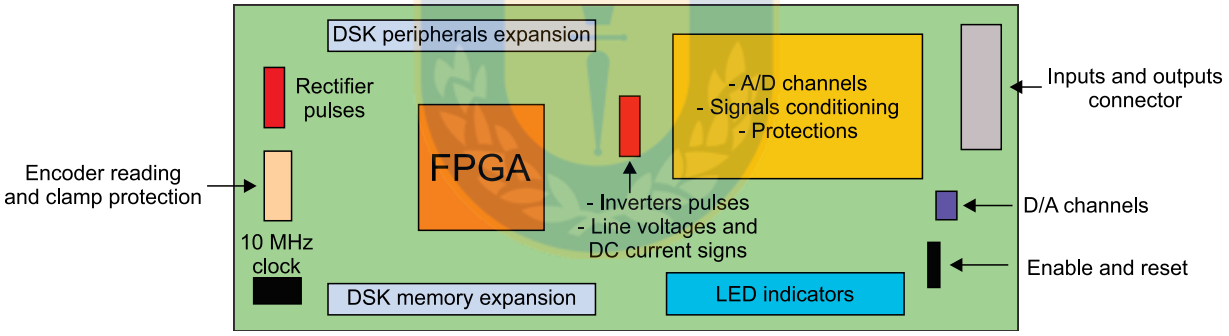


Fig. 4.10. Interface board structure diagram

The registers of the FPGA used to control the two-output IMC are shown in Appendix 2.

4.6. Voltage and current measurement

To measure the input voltages of the system, a board based on voltage transducers LEM LV25-P is used. These transducers are supplied with ±15 V and can measure up to 500 V. For the measurement, a 47 kΩ resistor is connected in series with the primary of the sensor to obtain a current proportional to the voltage. The rated primary and secondary currents are 10mA (RMS) and 25 mA (RMS), respectively. The conversion ratio of the transducer is 2500:1000. This type of

voltage transducer is also used in the DC link of the IMC for the over voltage protection circuit. The LV25-P transducer is shown in Fig. 4.11.

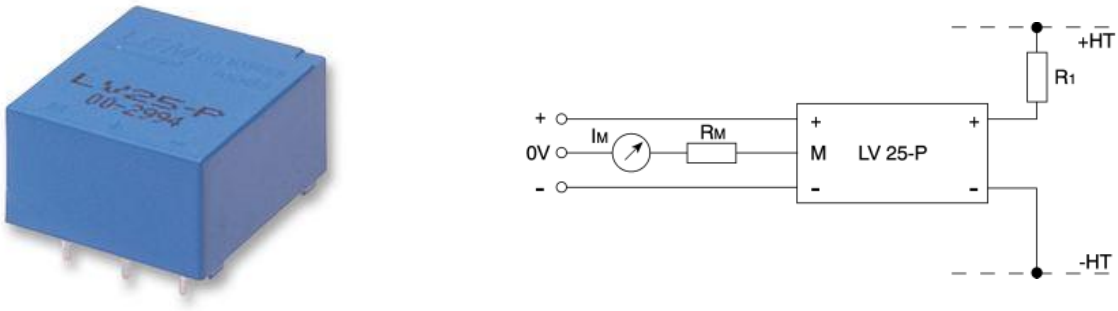


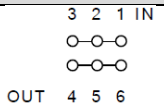
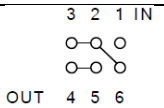
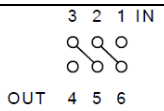
Fig. 4.11. Voltage transducer LV25-P and its connection

The current measurement board is built with for current transducer LEM LA55-P supplied with ±15 V. These transducers can measure currents up to 50 A (RMS). The transducer secondary current is proportional to the input current with a conversion ratio of 1:1000, then the secondary current can vary between 0 and 50 mA (RMS). The LA55-P current transducer is shown in Fig. 4.12.

Fig. 4.12. Current transducer LA55-NP and its connection

On the other hand, the current transducers installed in the outputs of the power converter are LEM LAH25-NP and are used to measure the machine phase currents. These transducers are supplied with ±15 V and allow a maximum primary and secondary currents of 25 A (RMS) and 25 mA (RMS), respectively. The LEM LAH25-NP has the capability of changing the conversion ratio which can have, depending on the pins configuration of the transducer, any of the following values: 1:1000, 2:1000 and 3:1000. Table 4.1 shows the connections and the rated current values for each conversion ratio. Fig. 4.13 shows the transducer LAH25-NP and its connection.

Table 4.1. Connections for changing the conversion ratio of the LAH25-NP current transducer

Primary turns	Rated primary current [A]	Rated secondary current [mA]	Conversion ratio	Recommended connections
1	25	25	1:1000	
2	12	24	2:1000	
3	8	24	3:1000	

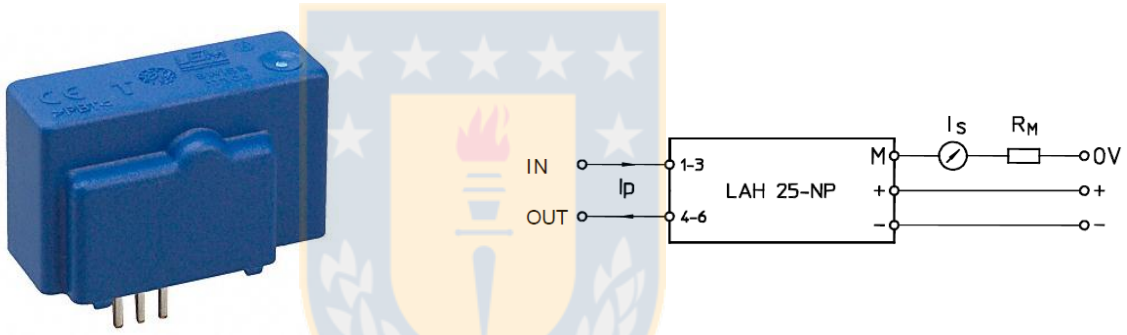


Fig. 4.13. Current transducer LAH25-NP and its connection

The schematic diagrams of the voltage and current measurement boards can be found in Appendix 4.

4.7. Encoder reading board

An incremental encoder with a resolution of 10000 ppr (pulses per revolution) is used to measure the rotor position of the induction machine. The encoder reading board is based on the differential receptor DS26LS32CN, which from the three differential signals provided by the encoder, produces three signals that are sent to the interface board. The encoder, manufactured by *British Encoder* is shown in Fig. 4.14 and a diagram of the encoder reading board connection is shown in Fig. 4.15.

Fig. 4.14. Incremental encoder

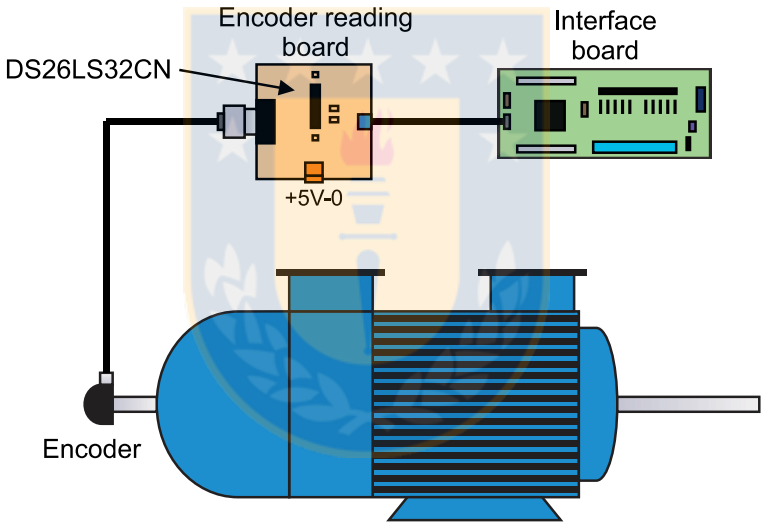


Fig. 4.15. Diagram of the encoder reading board connection

The schematic circuit of the encoder reading board can be seen in Appendix 4.

4.8. Direct current machine

A DC machine built by *Thrige Electric* is used as a separately excited generator coupled the induction motor shaft. The armature terminals of the DC generator are connected to a variable resistor then a variable load can be applied to the induction machine. The DC machine is shown in Fig. 4.16 and its plate information is summarized in Table 4.2.

Table 4.2. DC machine plate information

Power	6.5 kW
Speed	1510 rpm
Armature voltage	400 V
Armature current	20.2 A
Field voltage	340 V
Field current	1.3 A

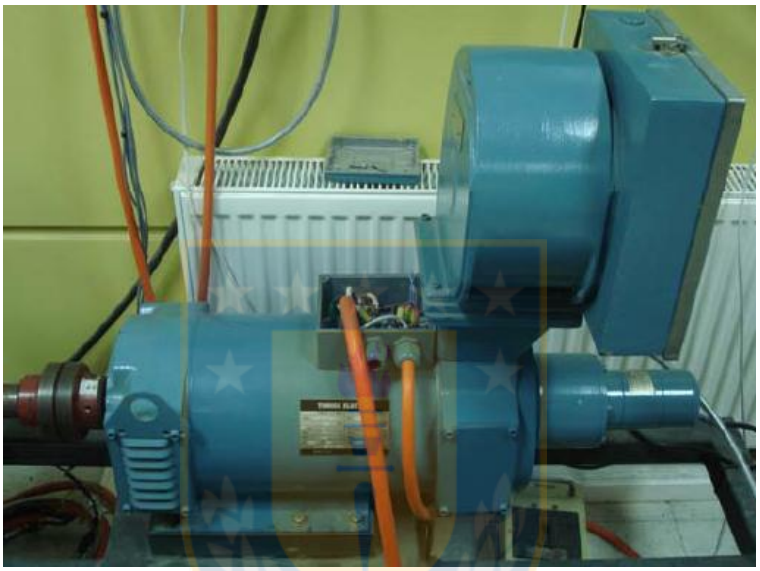


Fig. 4.16. DC generator

4.9. Induction machine

The AC motor used in open-end winding connection is a *Marelli Motori* wound rotor induction machine. For the purpose of the experimental implementation the motor is used with its rotor terminals short-circuited. The machine is shown in Fig. 4.17. Its plate information is given in Table 4.3 and its parameters are given in Table 4.4.

Table 4.3. Induction machine plate information

Power	7.5 kW	
Frequency	50 Hz	
Stator voltage	Δ	Y
	220 V	380 V
Stator current	Δ	Y
	30 A	17.5 A
Rotor voltage	250 V	
Rotor current	19 A	
Poles	6	
Speed	960 rpm	

Table 4.4. Induction machine parameters

Stator resistance	0.398 Ω (ref. to stator)
Stator inductance	0.0854 H (ref. to stator)
Rotor resistance	0.276 Ω (ref. to rotor)
Rotor inductance	0.0434 H (ref. to rotor)
Magnetizing inductance	0.0818 H (ref. to stator)

Fig. 4.17. Induction machine

4.10. Three-phase autotransformer

The indirect matrix converter is supplied by a three-phase autotransformer in order to have the possibility of applying a variable voltage to the system. The autotransformer is built by *Superior Electric* and is shown in Fig. 4.18. Its plate information is summarized in Table 4.5.

Table 4.5. Autotransformer plate information

Frequency	50 – 60 Hz
Maximum input voltage	480 V
Output voltage	0 – 560 V
Aparent power	27.2 kVA
Rated current	28 A

Fig. 4.18. Three-phase autotransformer

4.11. Experimental setup

Fig. 4.19 shows a diagram of the experimental system indicating the main connections between the different hardware elements.

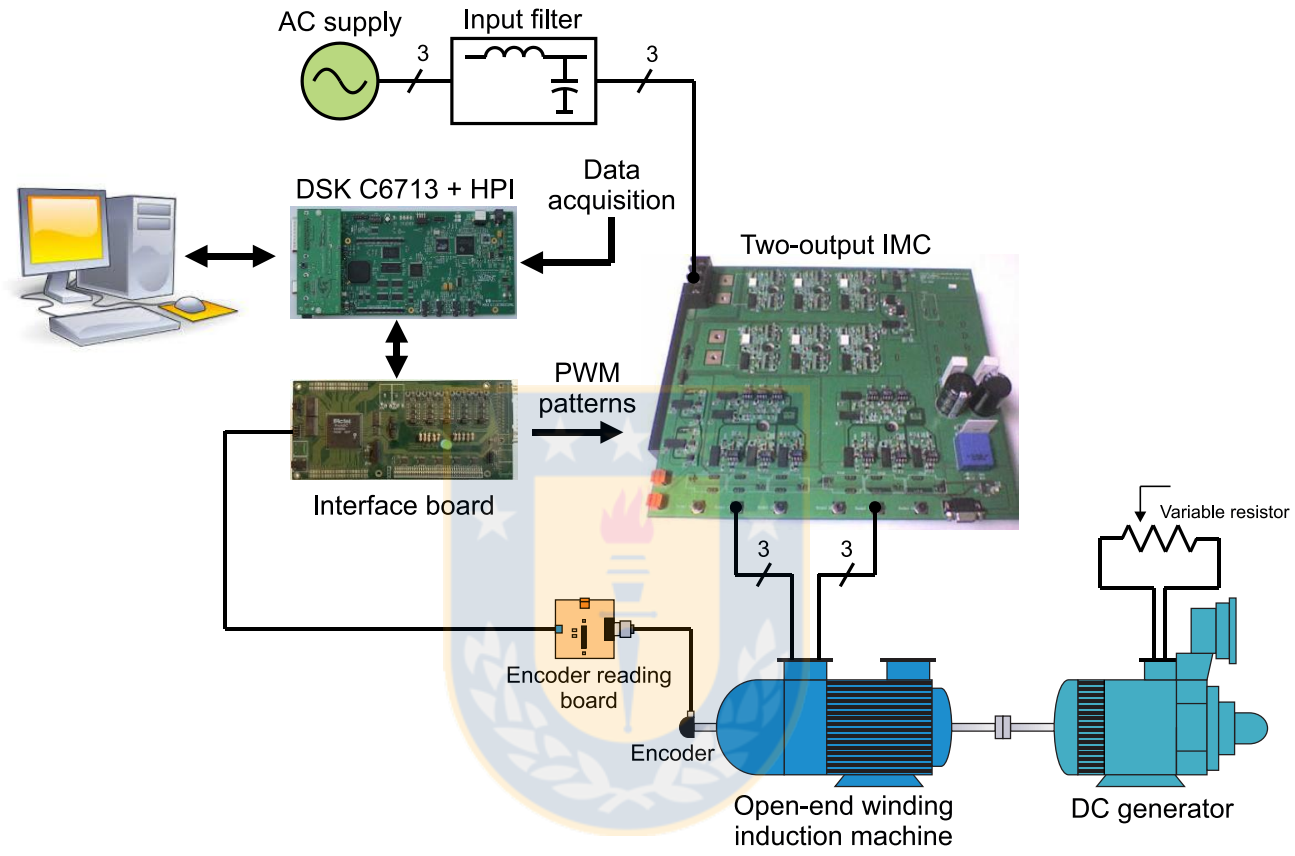


Fig. 4.19. Experimental setup diagram

The diagram of Fig. 4.19 is a general overview of the experimental system implemented in laboratory. This setup is used to obtain the experimental results to validate the thesis project which are shown in chapter 5.

Chapter 5. Simulation and Experimental Results

This chapter presents the simulation and experimental results obtained using the modulation strategies described in chapter 3. For simulation purposes PSIM platform is used to model the overall system (power and control stages) and the results are then plotted and analyzed in MATLAB. The experimental results have been obtained using the setup of Fig. 4.19 and the waveforms are either plotted in MATLAB or extracted directly from a oscilloscope.

5.1. Simulation results

The modulation strategies presented in chapter 3 are simulated in PSIM software. A flow diagram of the simulation method can be found in Appendix 1. The carrier-based PWM strategy and the SVM for common-mode voltage reduction in the IMC output stages are used in open-loop V/f operation of the induction machine along with the modulation for maximum DC voltage in the rectifier. The SVM strategy for zero sequence voltage reduction in the dual-inverter is used in closed-loop operation for vector control of the machine currents; the modulation strategies for reduced and maximum DC link voltage are used for the rectifier in this case.

In the simulation platform, the switches are considered ideal and dead times are neglected. The induction machine model considers the parameters shown in Table 4.4. Other simulation values of interest are presented in Table 5.1.

Table 5.1. Simulation parameters

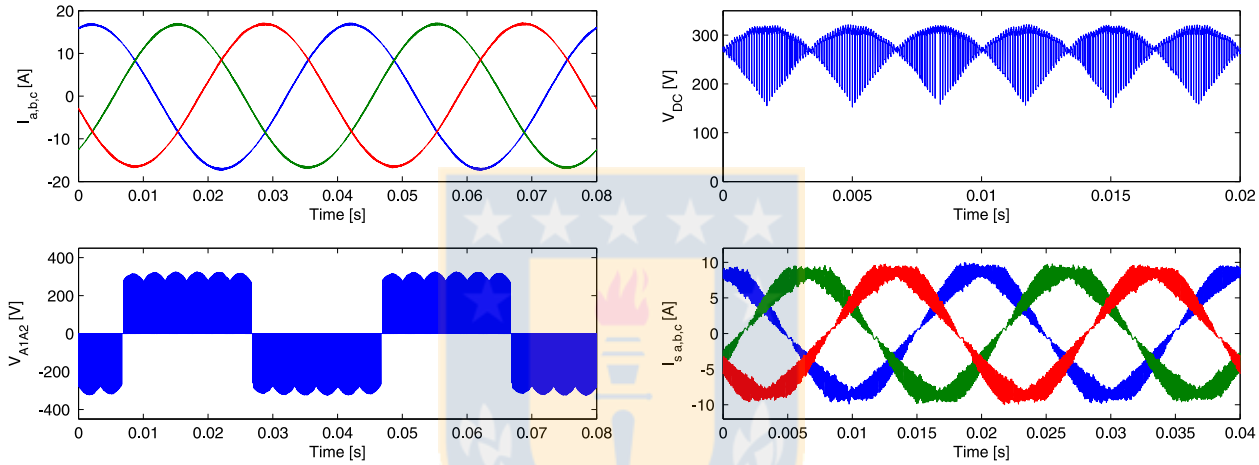
Variable	Description	Value
P_m	Machine power	7.5 kW
V_s	Input phase voltage	130 V
f	Input voltage frequency	50 Hz
f_s	Switching frequency	10 kHz
C_f	Input filter capacitance	2 µF
L_f	Input filter inductance	0.5 mH

5.1.1 Carrier-based modulation strategy

As mentioned above, the carrier-based PWM strategy for the output inverters of the IMC is used in open-loop V/f operation of the machine and the modulation for the input rectifier aims to

maximize the DC link voltage. Steady state results are shown for output frequencies of 25 and 50 Hz.

For an output frequency of 25 Hz, Fig. 5.1a shows the machine currents (top) and the machine phase-a voltage (bottom). Sinusoidal converter output currents can be appreciated. The DC link voltage is shown in Fig. 5.1b (top) while the converter input currents obtained are shown in Fig. 5.1b (bottom). The high frequency ripple content that can be noticed in the input currents could be reduced by modifying the converter input filter.



a) b)

Fig. 5.1. SPWM 25 Hz output. a) Machine currents (top) and output phase-a voltage (bottom). b) DC link voltage (top) and input currents (bottom)

As discussed in chapter 2, a zero sequence voltage could be applied to the open-end winding induction machine depending on the modulation strategy used for the dual-inverter. In this case, the carrier-based modulation strategy does generate a zero sequence voltage which is applied to machine phase windings (Fig. 5.2 top). However, as can be seen in Fig. 5.2 (bottom), this zero sequence voltage has only high frequency components then producing a negligible effect in the output currents (due to the inductive nature of the load). The zero sequence voltage has been obtained from the voltage across the load in each phase and then applying (2.32).

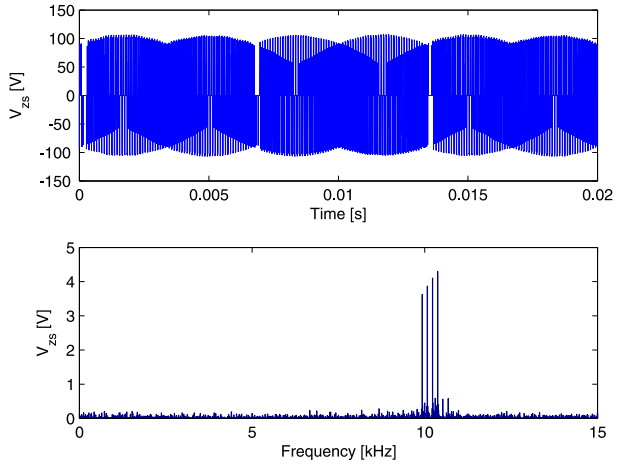
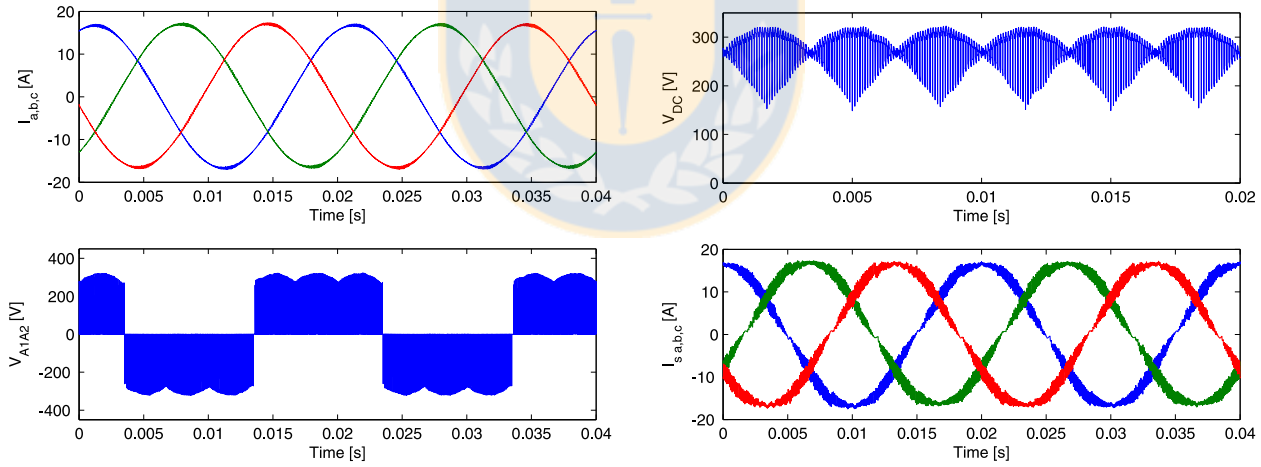


Fig. 5.2. Output zero sequence voltage (top) and its frequency spectrum (bottom) for 25 Hz output

If the output frequency of the converter is set to 50 Hz, the results obtained are shown in Fig. 5.3-5.4. Fig. 5.3a shows the machine currents (top) and the output phase-*a* voltage (bottom) while Fig. 5.3b shows the DC link voltage (top) and the converter input currents (bottom). It can be seen that the input currents present less ripple than the case of 25 Hz.



a) b)

Fig. 5.3. SPWM 50 Hz output. a) Machine currents (top) and output phase-*a* voltage (bottom). b) DC link voltage (top) and input currents (bottom)

The zero sequence voltage produced by the dual-inverter output of the converter is shown in Fig. 5.4 (top) and its frequency spectrum is shown in Fig. 5.4 (bottom). Again the zero sequence voltage presents only high frequency components but in this case of larger amplitude than the case of 25 Hz output.

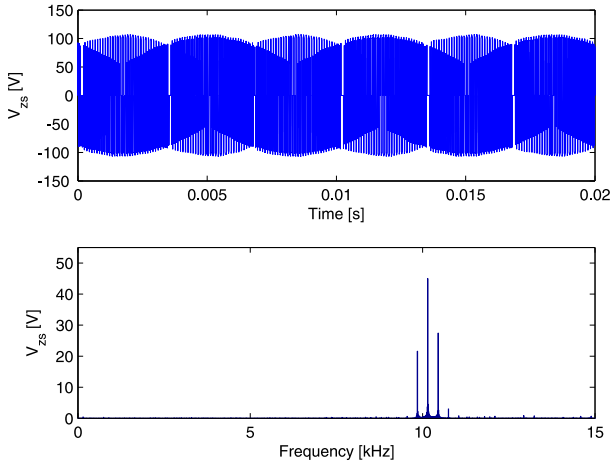


Fig. 5.4. Output zero sequence voltage (top) and its frequency spectrum (bottom) for 50 Hz output

As commented in chapter 3, the carrier-based modulation strategy does not address the issue of common-mode voltage. The generated common-mode voltages v_{cm0} and v_{0G} are shown in Fig. 5.5 top and middle, respectively. Due to absence of the reference point 0 in the real (and also simulated) converter, the common-mode voltages v_{0G} and v_{cm0} are obtained as:

$$v_{cm0} = \frac{1}{6}(v_{A1n} + v_{B1n} + v_{C1n} + v_{A2n} + v_{B2n} + v_{C2n}) - \frac{v_{DC}}{2} \tag{5.1}$$

$$v_{0G} = v_{nG} + \frac{v_{DC}}{2} \tag{5.2}$$

where n is the negative rail of the DC link.

On the other hand, the converter input rectifier is modulated to operate with unity displacement factor at the input; this can be seen in Fig. 5.5 (bottom) where the input phase-a voltage and current are shown.

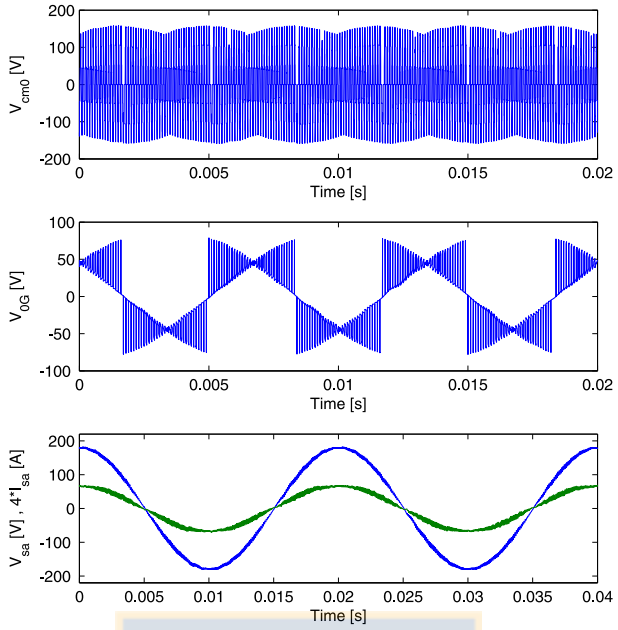


Fig. 5.5. Common-mode voltages v_{cm0} (top) and v_{0G} (middle). Input phase-a voltage and current (bottom)

It should me mentioned that the waveforms presented in Fig. 5.5 top and middle are valid for any output frequency of the power converter. The unity input displacement factor is always achieved but the input current of Fig. 5.5 (bottom) could have more or less distortion depending on the output frequency.

5.1.2 SVM for zero sequence voltage reduction

The SVM strategy for zero sequence voltage reduction is used in an indirect feedforward vector control scheme for the machine currents. The modulation strategies for reduced and maximum DC link voltage are used for the rectifier depending on the output voltage requirement. A diagram of the control scheme is shown in Fig. 5.6.

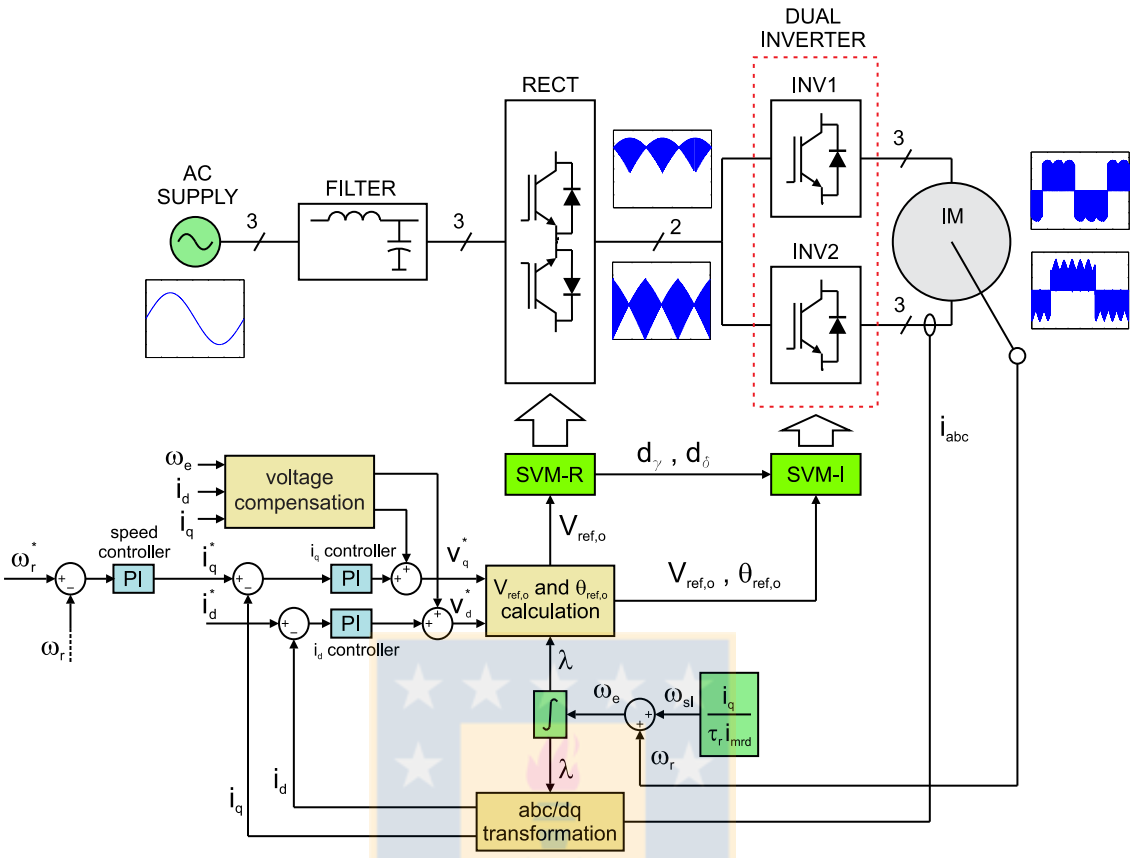


Fig. 5.6. Feedforward vector control scheme of an open-end winding induction machine

The PI current controllers are designed aiming for a natural frequency $f_o = 70\,Hz$ and a damping coefficient $\xi = 0.8$. To obtain a preliminary design of the dq current control loops, the diagram of Fig. 5.7 is used, where K_p and K_i are the proportional and integral constants of the PI current controller, R_s is the stator resistance, L_s the stator self-inductance and σ is a total leakage coefficient given by $\sigma = 1 - L_o^2/L_sL_r$, with L_o the magnetizing inductance and L_r the rotor self-inductance of the machine. The parameters of the machine are given in Table 4.4.

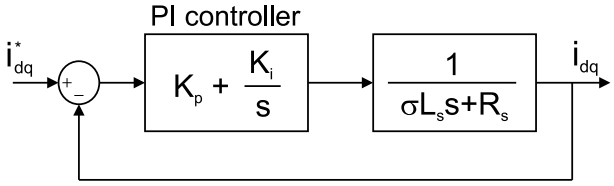


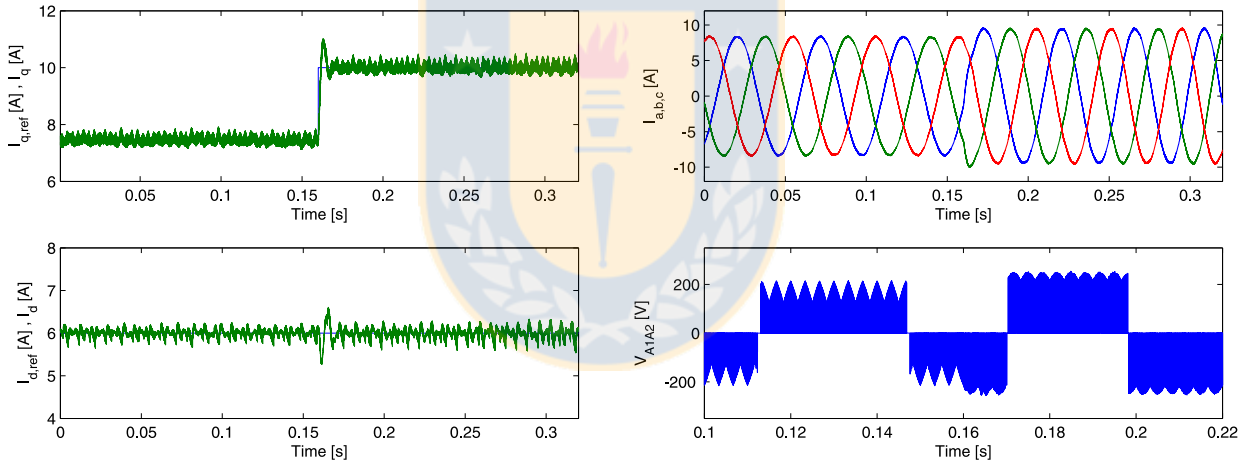
Fig. 5.7. Block diagram for *dq* currents control design

For implementation purposes the PI current controller designed is discretized using zero-order hold discretization method. The resultant discrete controller is:

$$G_c(z) = K_p + \frac{K_i T_s}{z-1} \tag{5.3}$$

where T_s is the sampling time (0.1 ms).

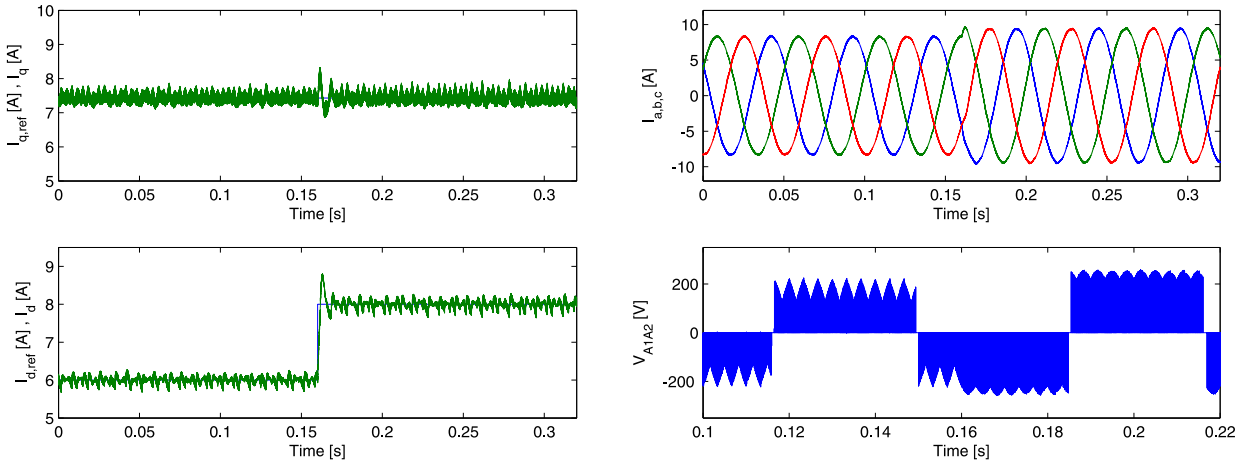
The performance of the vector control scheme is verified by applying step changes in the *dq*-axis reference currents. Fig. 5.8 – 5.9 show the waveforms obtained by applying a step change in the *q*-axis reference current from 7.7 A to 10 A at $t = 0.16\ s$, while *d*-axis current is kept constant at 6 A. Fig. 5.8a shows *dq* reference currents and their corresponding responses. As can be observed good tracking of the reference currents is obtained. The motor currents and phase-*a* voltage are shown in Fig. 5.8b. The step change in *q*-axis current is followed with changes in the magnitude and phase of the instantaneous machine currents. Moreover, a transition between reduced virtual DC voltage to maximum virtual DC voltage can be noticed in the output phase voltage of Fig. 5.8b (bottom).



a) b)

Fig. 5.8. *q*-axis current step change. a) Motor *q*-axis current (top) and *d*-axis current (bottom). b) Motor currents (top) and phase voltage (bottom)

Fig. 5.9a shows the performance of the control scheme when a step change from 6 A to 8 A is applied in *d*-axis reference current while *q*-axis current is kept constant at 7.7 A. The motor currents and phase-*a* voltage are shown in Fig. 5.9b. Again the transition between both modulation strategies for the input rectifier can be noticed.



a) b)

Fig. 5.9. *d*-axis current step change. a) Motor *q*-axis current (top) and *d*-axis current (bottom). b) Motor currents (top) and phase voltage (bottom)

Fig. 5.10 (top) shows the converter input phase voltage and current; the unity input displacement factor can be noted. Fig. 5.10 (bottom) shows the output zero sequence voltage. As can be seen, the zero sequence voltage has been eliminated due to the modulation strategy used for the output stages.

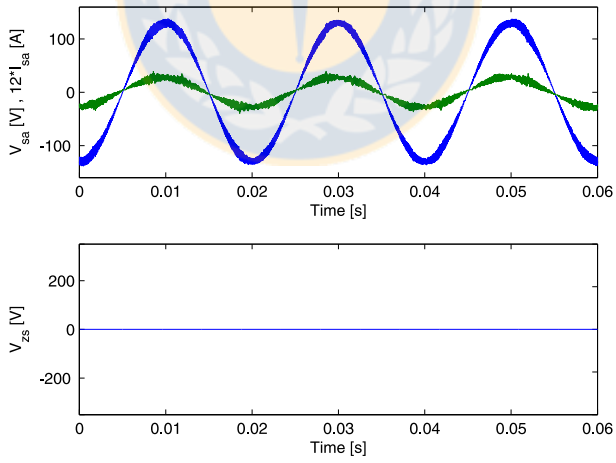


Fig. 5.10. Input phase voltage and current (top) and zero sequence voltage (bottom)

The elimination of the zero sequence voltage is theoretical. In a real system, due to power devices dead times and turn-on times there will not be an elimination but a reduction of the zero sequence voltage.

5.1.3 SVM for common-mode voltage reduction

The SVM strategy intended to reduce the common-mode voltage is used in open-loop V/f operation to control the machine. The modulation strategy used for the input stage of the power converter aims to maximize the DC link voltage. The occurrence of low frequency zero sequence voltage is avoided by performing the compensation commented in section 3.2.3. For simulation purposes, the load used is a constant torque, set to 30 Nm.

The DC link voltage and phase-a machine voltage are shown in Fig. 5.11, top and bottom, respectively. The reference output voltage and frequency were set to 150 V and 50 Hz respectively.

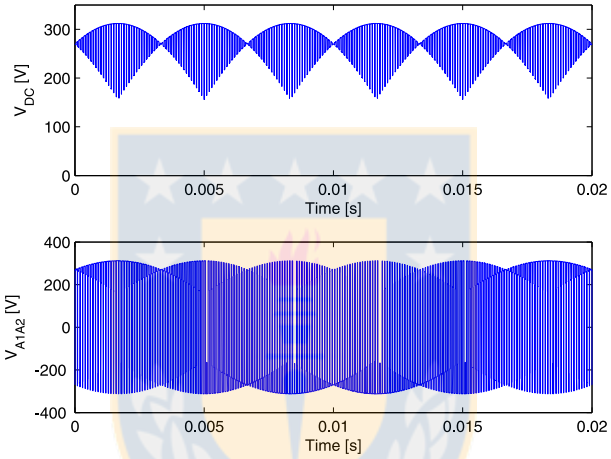


Fig. 5.11. DC link voltage (top) and output phase voltage (bottom)

The machine currents for 25 Hz operation are shown in Fig. 5.12 (top), while Fig. 5.12 (bottom) shows machine currents for 50 Hz operation.

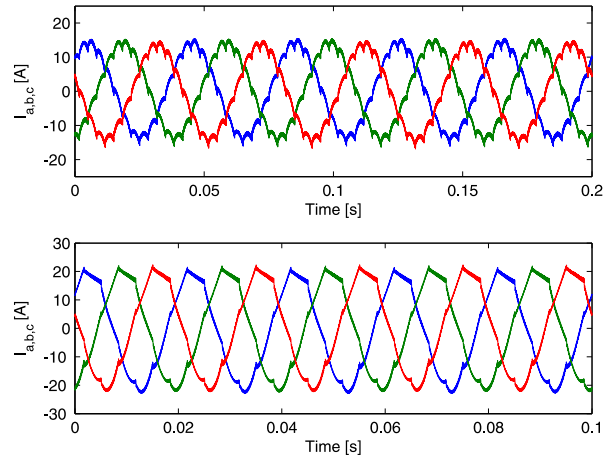


Fig. 5.12. Machine currents for 25 Hz output (top) and 50 Hz output (bottom)

Small disturbances, occurring every 60°, can be noted in the motor currents shown in Fig. 5.12. These current disturbances are due to the application of zero voltage vectors to machine windings, see PWM pattern in Fig. 3.11, aiming to reduce the zero sequence voltage. During the application of zero voltage vectors each machine phase winding is supplied with a voltage of $-V_{DC}$ or $+V_{DC}$. When $-V_{DC}$ voltage is applied to the machine windings the current decreases according to the zero vector duty cycle. Fig. 5.13 shows the current disturbance along with the corresponding DC link voltage and output phase voltage.

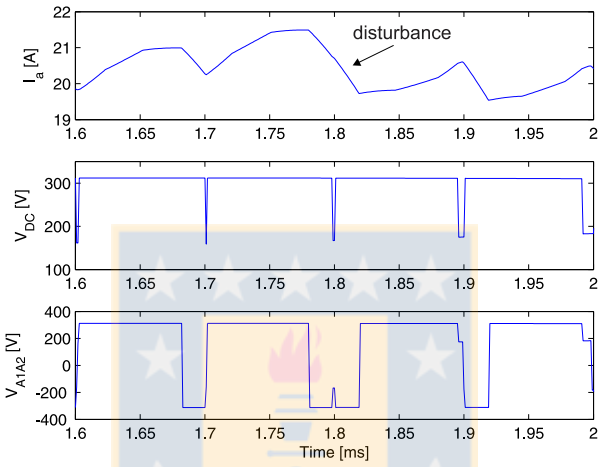


Fig. 5.13. Phase a machine current (top), DC link voltage (middle) and machine phase-a voltage (bottom)

The low order harmonics of the machine currents are presented in Table 5.2.

Table 5.2. Harmonic content of the machine currents

Current Harmonic	RMS Value [A]
Fundamental	14.400
2nd	0.250
3rd	0.184
4th	0.112
5th	0.025
6th	0.815

The input (supply) currents are shown in Fig. 5.14 (top) while Fig. 5.14 (bottom) shows the converter input phase voltage (blue) and current (green) for an output reference of 150 V and 50 Hz. The unity displacement factor is evident in Fig. 5.14 (bottom).

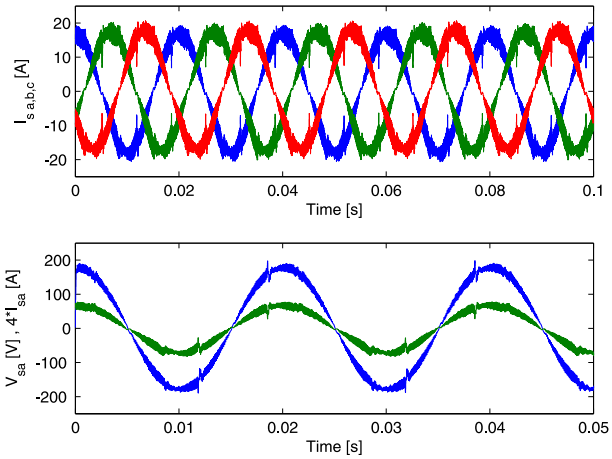


Fig. 5.14. Input currents (top) and input phase voltage and current (bottom)

Fig. 5.15 shows the common-mode voltage separated into v_{0G} and v_{cm0} as defined in (2.46). It can be seen in the simulation results that the contribution of the output inverters to the common-mode voltage is completely eliminated due to the modulation strategy used.

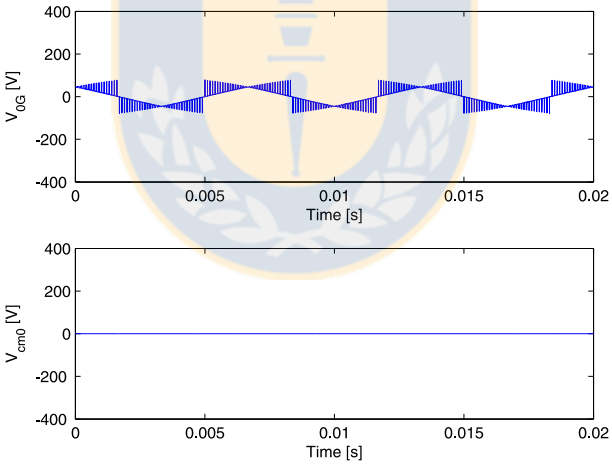


Fig. 5.15. Common-mode voltages v_{0G} (top) and v_{cm0} (bottom)

Fig. 5.16 shows the zero sequence voltage (top) and its frequency spectrum (bottom). It can be noted that the low order zero sequence harmonics are reduced because of the asymmetry of the null vector duty cycles used in the switching sequence for each output stage.

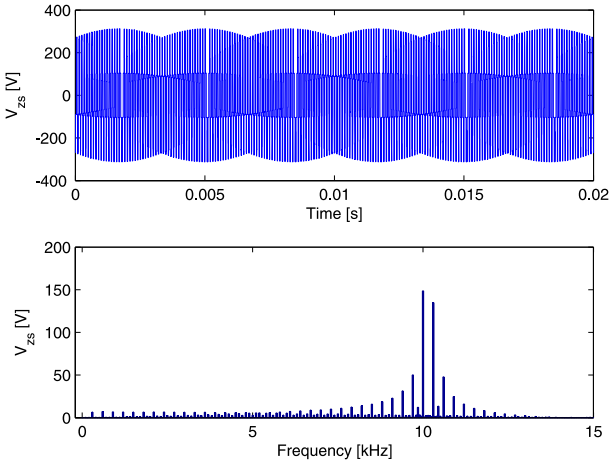


Fig. 5.16. Zero sequence voltage (top) and its frequency spectrum (bottom)

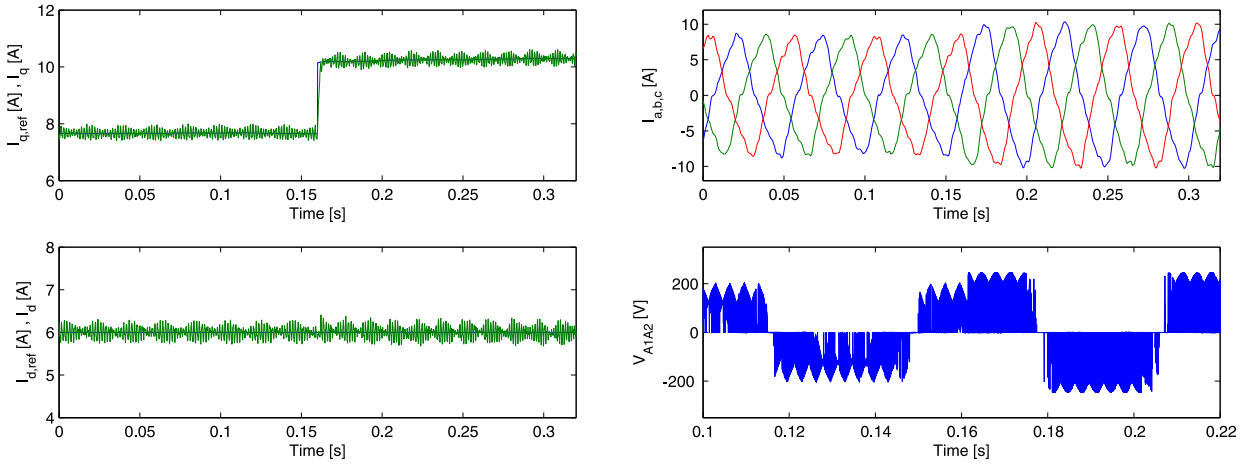
5.2. Experimental results

The SVM strategies aiming to reduce the zero sequence voltage and the common-mode voltage are tested in the laboratory setup shown in Fig. 4.19 in order to obtain experimental results and validate the simulations shown in sections 5.1.2 and 5.1.3. The sampling frequency used for measuring voltages and currents is 10 kHz. The parameters of the experimental system are the same used in the simulation platform (Table 5.1). The main parts of the C codes programmed on the DSP board to implement the modulation strategies are shown in Appendix 3.

5.2.1 SVM for zero sequence voltage reduction

As in the simulation results of section 5.1.2, the SVM strategy to reduce the zero sequence voltage is used in a vector control scheme for the machine currents (Fig. 5.6). The input rectifier can use either the SVM to maximize or reduce the DC link voltage.

The *dq*-axis currents are shown in Fig. 5.17a. As the speed controller saturates when a step change in the speed reference takes place, a step change in *q*-axis current reference is applied. The *d*-axis current reference is kept constant at 6 A. A good performance of the control scheme can be appreciated agreeing with the simulation results. The motor instantaneous currents and phase-*a* voltage are shown in Fig. 5.17b. The transition between both rectifier modulation strategies can be noted in the output phase voltage (Fig. 5.17b bottom) when the change in *q*-axis reference current is applied.

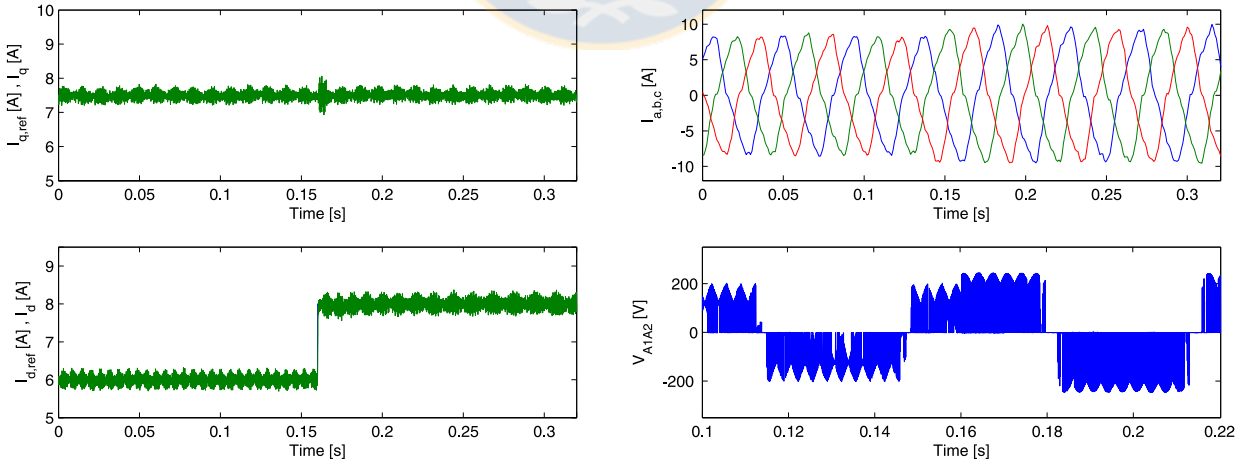


a) b)

Fig. 5.17. *q*-axis current step change. a) Motor *q*-axis current (top) and *d*-axis current (bottom). b) Motor currents (top) and phase voltage (bottom)

Fig. 5.18a shows the *dq* machine currents when a step change in *d*-axis reference current is applied while *q*-axis current is kept constant at 7.7 A. The motor currents and phase-*a* voltage are shown in Fig. 5.18b. A good correspondence with the simulation results can be noted.

Finally, Fig. 5.19 (top) shows the input phase voltage and current. The zero sequence voltage is shown in Fig. 5.19 (bottom).



a) b)

Fig. 5.18. *d*-axis current step change. a) Motor *q*-axis current (top) and *d*-axis current (bottom). b) Motor currents (top) and phase voltage (bottom)

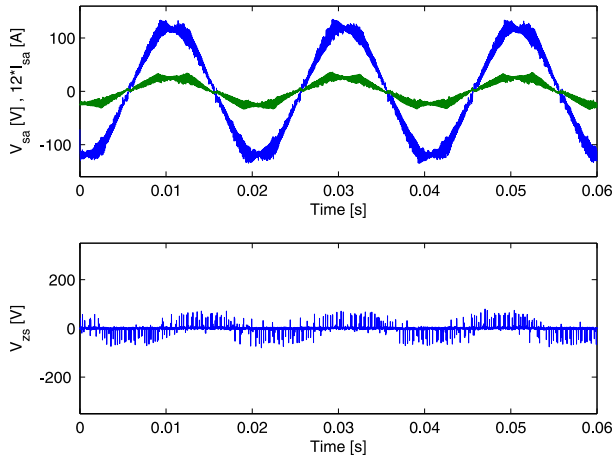


Fig. 5.19. Input rectifier voltage and current (top) and zero sequence voltage (bottom)

As can be noted, the zero sequence voltage is not exactly zero but this is probably due to the measurement procedure because not all of the channels are sampled at the same time and because in Fig. 5.10 the input switches are ideal.

5.2.2 SVM for common-mode voltage reduction

The modulation strategy for common-mode voltage reduction is used in open-loop V/f operation for the induction machine. The rectifier is modulated to maximize the DC link voltage. To avoid the circulation of low frequency zero sequence currents in the machine windings, the null vectors are applied with unequal duty cycles (Fig. 3.11) according to the compensation proposed in section 3.2.3.

Fig. 5.20 (top) shows the DC link voltage while Fig. 5.20 (bottom) shows the voltage across the machine phase-a winding. The output phase voltage presents a fundamental component of 141 V, 50 Hz, slightly less than the voltage reference (150 V) because of the device voltage drops. As can be seen the modulation strategy used results in a bipolar pulse width modulated voltage at the converter output. Correspondence between the simulations of section 5.1.3 and the experimental results can be observed.

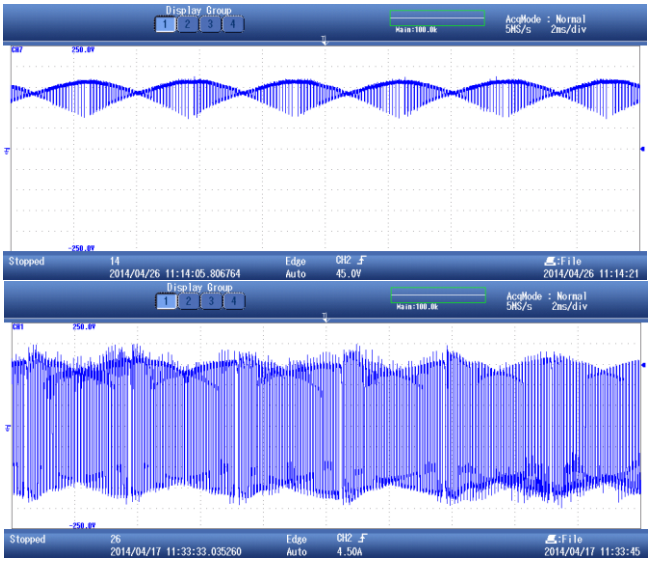


Fig. 5.20. DC link voltage (top) and output phase voltage (bottom)

The machine currents for 25 Hz and 50 Hz operation are shown in Fig. 5.21 top and bottom, respectively. The reference output voltages are set to 75 V and 150 V, respectively.

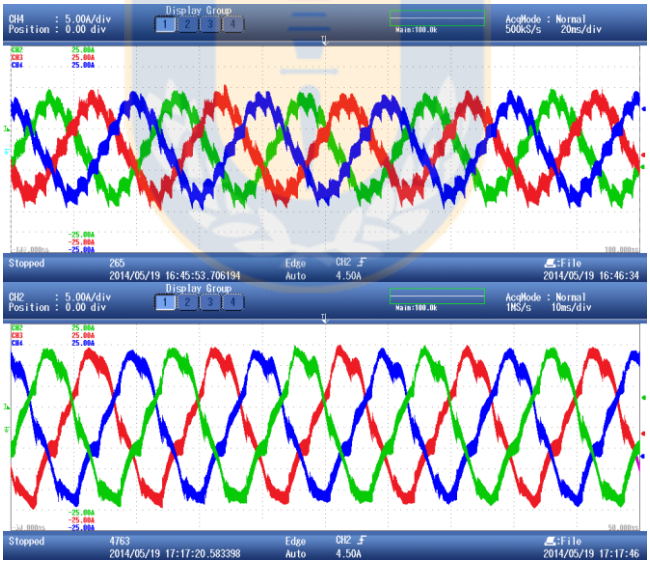


Fig. 5.21. Machine currents for 25 Hz output (top) and 50 Hz output (bottom)

In Fig. 5.21, the effect of the zero voltage vectors in the PWM pattern shown in Fig. 3.11 is also observed. The supply currents are shown in Fig. 5.22 (top), again with good correspondence with the simulation study. Fig. 5.22 (bottom) shows the input phase voltage and current.

Fig. 5.23 shows the common-mode voltages v_{0G} (top) and v_{cm0} (bottom). The voltage v_{0G}

follows very closely the simulation results shown in Fig. 5.15. The voltage v_{cm0} is not exactly zero due to the non-ideal characteristics of the real switches in comparison to those used in the simulations.

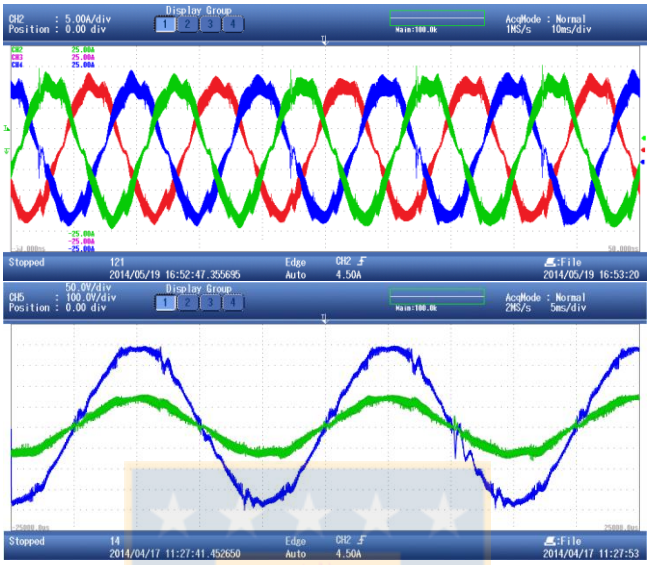


Fig. 5.22. Input currents (top) and input phase voltage and current (bottom)

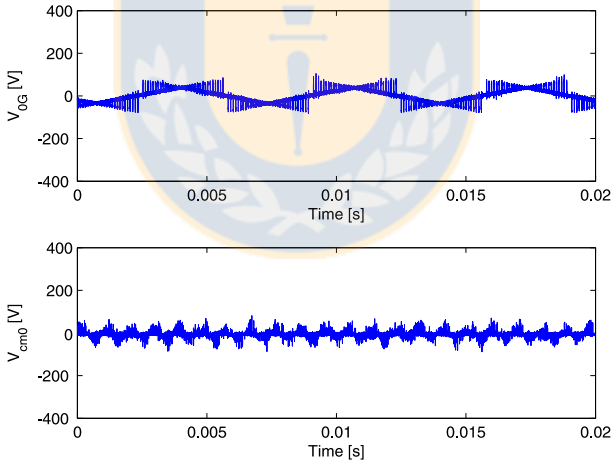


Fig. 5.23. Common-mode voltages v_{0G} (top) and v_{cm0} (bottom)

Finally, Fig. 5.24 shows the zero sequence voltage (top) and its frequency spectrum (bottom), agreeing closely with the simulation results.

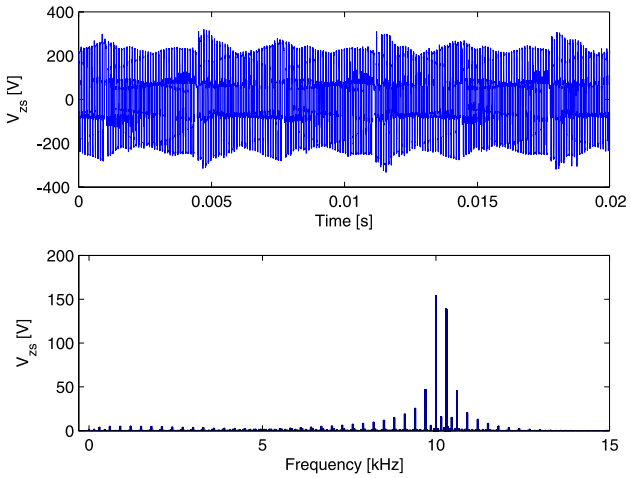


Fig. 5.24. Zero sequence voltage (top) and its frequency spectrum (bottom)

Due to the compensation performed in the switching strategy, the zero sequence voltage has only high frequency components then the effect on the output currents is negligible.

Chapter 6. Conclusions

This thesis has presented a topology consisting of an indirect matrix converter with two output stages to supply energy to an open-end winding induction machine. The input and output stages of the power converter can be controlled in order to achieve certain voltage/current characteristics in both ends (input/output) of the IMC. The advantages of an open-end winding connection in comparison to a standard wye or delta connected machines have been outlined, being the most important the possibility of reducing the common-mode voltage of the system. On the other hand the main disadvantage of an open-end winding topology is that a zero sequence voltage can be generated by the power converter output producing a zero sequence current that circulates in the machine windings.

Different modulation strategies have been presented for the input and output stages of the IMC. The modulation strategies have been tested via computer simulations in PSIM and verified experimentally in a 7.5 kW laboratory prototype. For the IMC input rectifier two SVM strategies have been shown. Depending on the output voltage requirement, the rectifier can be modulated in order to maximize the DC link voltage or to produce a reduced DC link voltage. The generation of a maximum DC voltage allows maximizing the voltage gain of the power converter. The generation of a reduced DC voltage allows the input and output stages of the IMC to commutate with lower voltage thus reducing the switching losses. Moreover, regardless of the modulation strategy used for the rectifier, the converter can operate with unity input displacement factor.

For the dual-inverter output, three modulation strategies have been presented. The first one is a unipolar carrier-based modulation strategy, a standard technique used in power converters. This PWM strategy produces zero sequence voltage at the machine terminals. However the zero sequence voltage produced contains only high frequency component, then the effect on the machine currents is negligible. The carrier-based PWM strategy was tested in a simulation platform where low distorted input currents can be appreciated. This modulation method does not address the issue of the common-mode voltage in the open-end winding machine.

The second PWM strategy, SVM, is intended to reduce the zero sequence voltage at the machine terminals. This strategy is based on the space voltage vectors available in the dual-inverter that do not produce zero sequence voltage. Moreover, it has been shown that there are two equivalent set of vectors available for zero sequence voltage reduction. This redundancy could be

useful for operating in a fault tolerant open-end winding machine drive. This modulation method was used, along the SVM strategies presented for the rectifier, in an indirect feedforward vector control scheme for the machine currents. A good performance of the closed-loop control strategy was verified for step changes in the *dq*-axis reference currents. Independent of any dynamic response of the machine currents or the modulation strategy used for the rectifier, the zero sequence voltage at the machine windings is reduced due to the voltage vectors used in the converter output stages. For this modulation and control scheme an agreement between the simulation and experimental results presented has been obtained.

The third modulation strategy shown for the IMC dual-inverter output is a SVM intended to reduce the common-mode voltage of the system. The strategy consists on using only those voltage space vectors available in the output stages that do not produce common-mode voltage. It has been shown that vectors of different amplitudes achieve this objective. Moreover, there is redundancy for the shortest space vectors available. On the other hand, since the output voltage vectors that reduce the common-mode voltage do produce zero sequence voltage, compensation has been used in order to avoid the circulation of low order triplen harmonic currents in the machine windings. The compensation is based on applying null vectors of the dual-inverter with unequal duty cycles in each switching period. The calculation of the null vectors duty cycles is performed in every sampling period and aims to reduce the zero sequence volt-seconds in the output. The result is an output voltage that contains high frequency zero sequence components then the effect on the machine currents is negligible. A drawback of this modulation strategy is that, unlike standard SVM for VSIs, the null voltage vectors apply non-zero voltage in the output, then is not possible to commutate the input stage of the IMC with zero current and the switching losses will be higher than the case of the other modulation strategies presented. Moreover, the fact of having output voltage when the null vectors are applied implies a distortion in the machine currents that has been discussed in chapter 3. The modulation strategy for common-mode voltage reduction was tested for open-loop V/f operation of the machine in the simulation platform and the experimental rig.

The research carried out in this thesis project was focused upon the feasibility of using a two-output indirect matrix converter to supply an open-end winding induction machine. This has resulted in six conference publications [73]-[78] with [73] and [78] selected among the best papers of the Chilean Automatic Control Association (ACCA) Conference 2012 and the European Conference on

Power Electronics and Applications (EPE) 2015, respectively; and one journal publication [79] with two journal publications currently under revision and another in preparation.

Appendix 1. Simulation scheme

A general flow diagram of the simulations performed in PSIM platform is shown in Fig. A1.1.

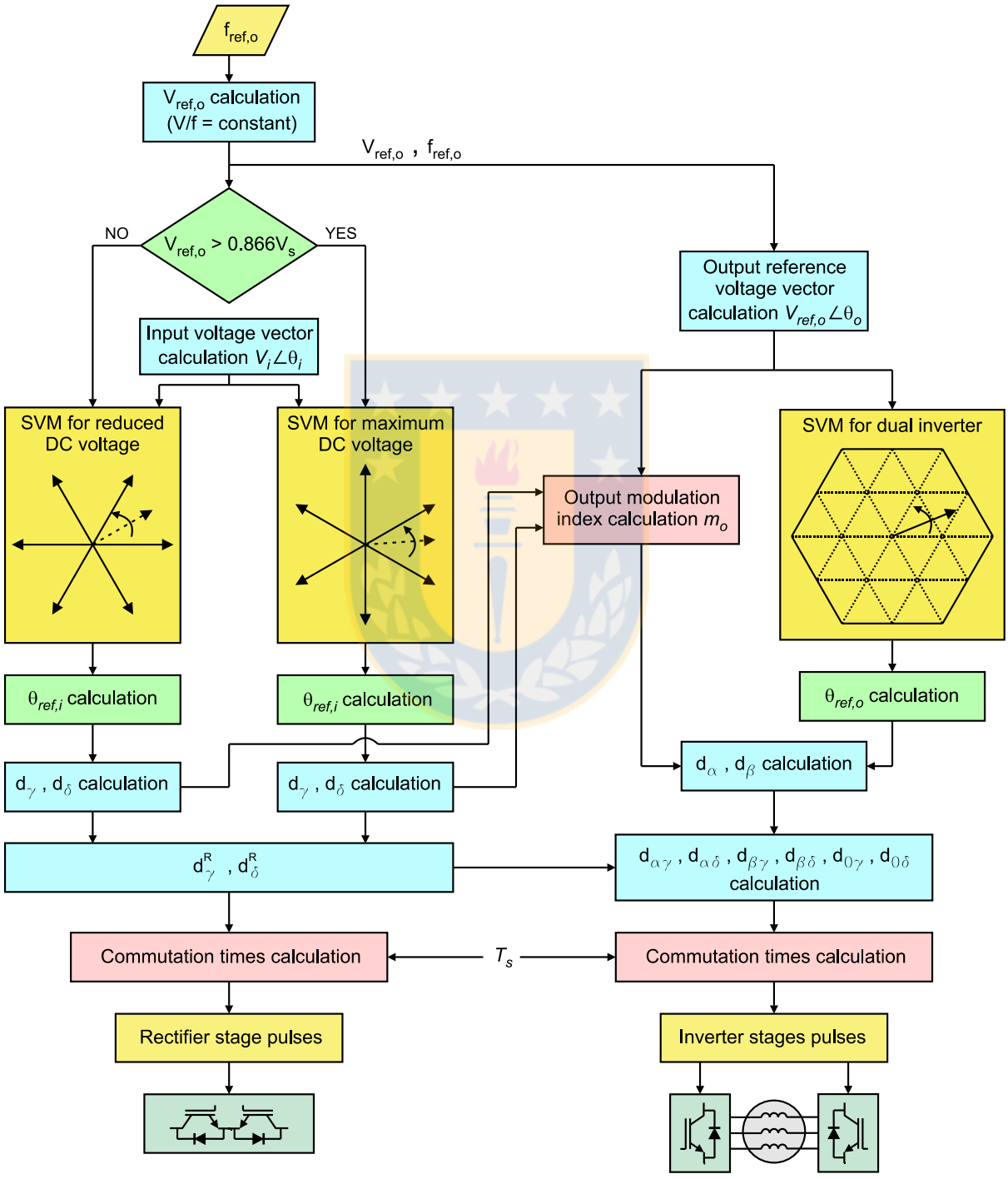


Fig. A1.1. Flow diagram of the simulation scheme

Appendix 2. FPGA registers

Table A2.1. Interface board FPGA registers

Register	Memory Address	Main features of the register
DPR0	0xA0000000	▪ Commutation period (16 bits). ▪ PWM reset (1 bit). ▪ PWM enable (1 bit). ▪ Interruption enable (1 bit).
DPR1	0xA0000004	▪ Rectifier stage vector (4 bits). ▪ Rectifier stage vector time (12 bits). ▪ Input line voltage sign (3 bits)
DPR2	0xA0000008	▪ Four-step commutation time, divided in three delays (10 bits each)
DPR3	0xA000000C	▪ A/D converter reading, channels 0 and 1 (16 bits each). ▪ Inverter 1 vector (4 bits). ▪ Inverter 1 vector time (12 bits).
DPR4	0xA0000010	▪ A/D converter reading, channels 2 and 3 (16 bits each). ▪ Inverter 2 vector (4 bits). ▪ Inverter 2 vector time (12 bits).
DPR5	0xA0000014	▪ A/D converter reading, channels 4 and 5 (16 bits each).
DPR6	0xA0000018	▪ A/D converter reading, channels 6 and 7 (16 bits each).
DPR7	0xA000001C	▪ A/D converter reading, channels 8 and 9 (16 bits each).
DPR8	0xA0000020	▪ Hardware trips reading (24 bits).
DPR9	0xA0000024	▪ Rectifier outputs enable (2 bits). ▪ Inverter 1 outputs enable (3 bits). ▪ Inverter 2 outputs enable (3 bits). ▪ Voltage/current commutation (1 bit).
DPR10	0xA0000028	▪ Inverters PWM buffers.
DPR11	0xA000002C	▪ Timers based on the FPGA clock frequency.
DPR12	0xA0000030	▪ Hardware trips enable (24 bits). ▪ Inverters dead times (8 bits).
DPR13	0xA0000034	▪ Encoder 1 instantaneous reading (16 bits).
DPR14	0xA0000038	▪ Encoder 2 instantaneous reading (16 bits).

Appendix 3. DSP programs

The main parts of the C codes programmed on the DSP board to implement the modulation strategies proposed are shown below.

A3.1. Rectifier modulation strategies

```
/* Angles calculation */
theta_R = atan2sp(Vbeta,Valfa;
theta_R=((theta_R<0)?(theta_R+two_pi):theta_R);
sector_R=(theta_R+pi_2)/pi_3;
sector_R=((sector_R==7)?1:sector_R);
offset_angle_R=(sector_R-1)*pi_3;
angle_sector_R=theta_R-offset_angle_R+0.5*pi_3;
angle_sector_R=((angle_sector_R>two_pi)?(angle_sector_R-two_pi):angle_sector_R);

/* Duty cycles for maximum DC voltage */
d_gamma=sinsp(pi_3-angle_sector_R);
d_delta=sinsp(angle_sector_R);
d_gammaR=d_gamma/(d_gamma+d_delta);
d_deltaR=1.0-d_gammaR;

/* Duty cycles for reduced DC voltage */
d_gamma=cossp(angle_sector_R_b);
d_delta=cossp(pi_3-angle_sector_R_b);

/* Condition to avoid negative DC voltage */
if (angle_sector_R_b<=0.034906585){ //2 degrees
    d_delta=0;
}
else if (angle_sector_R_b>=1.012290966){ //58 degrees
    d_gamma=0;
}

d_gammaR=d_gamma/(d_gamma+d_delta);
d_deltaR=1.0-d_gammaR;

/* Vectors and times */
d_gamma_time=(float)((0x3e7)*d_gammaR);
i=(sector_R-1)*2;
vector1=vectores[i];
vector2=vectores[i+1];

/* Vectors and times loading */
if (d_gamma_time<2)
    *dpr1=(vector2|(0x00));
else{
    *dpr1=(vector1|(d_gamma_time));
    *dpr1=(vector2|(0x00));
}
```

A3.2. Dual-inverter modulation strategies

A3.2.1 SVM for zero sequence voltage reduction

```
V_ref=220*f_ref/f_base; //output reference voltage
w=two_pi*f_ref;
m=V_ref/220; //modulation index


/* Reference angle calculation */
theta_i=theta_i+w*Dt;
theta_i=((theta_i>two_pi)?(theta_i-two_pi):theta_i);

/* Sector calculation */
sector_i=(theta_i+pi_3)/pi_3;
sector_i=((sector_i==7)?1:sector_i);

offsetangle_i=(sector_i-1)*pi_3;
theta_ref_i=theta_i-offsetangle_i;

/* Duty cycles */
d_alpha=(d_gamma+d_delta)*m*sinsp(pi_3-theta_ref_i);
d_beta=(d_gamma+d_delta)*m*sinsp(theta_ref_i);

/* Vectors selection depending on the sector */
if (sector_i==1){
    vect11=vector_inv[1]; vect12=vector_inv[4];
    vect21=vector_inv[2]; vect22=vector_inv[4];
    vect01=vector_inv[4]; vect02=vector_inv[4];
}
else if (sector_i==2){
    vect11=vector_inv[2]; vect12=vector_inv[4];
    vect21=vector_inv[2]; vect22=vector_inv[1];
    vect01=vector_inv[2]; vect02=vector_inv[2];
}
else if (sector_i==3){
    vect11=vector_inv[2]; vect12=vector_inv[1];
    vect21=vector_inv[4]; vect22=vector_inv[1];
    vect01=vector_inv[1]; vect02=vector_inv[1];
}
else if (sector_i==4){
    vect11=vector_inv[4]; vect12=vector_inv[1];
    vect21=vector_inv[4]; vect22=vector_inv[2];
    vect01=vector_inv[4]; vect02=vector_inv[4];
}
else if (sector_i==5){
    vect11=vector_inv[4]; vect12=vector_inv[2];
    vect21=vector_inv[1]; vect22=vector_inv[2];
    vect01=vector_inv[2]; vect02=vector_inv[2];
}
else{
    vect11=vector_inv[1]; vect12=vector_inv[2];
    vect21=vector_inv[1]; vect22=vector_inv[4];
    vect01=vector_inv[1]; vect02=vector_inv[1];
}
```

```
/* Combined duty cycles */
d_alpha_gamma=d_alpha*d_gamma_R;
d_alpha_delta=d_alpha*d_delta_R;
d_beta_gamma=d_beta*d_gamma_R;
d_beta_delta=d_beta*d_delta_R;
d0=1-(d_alpha+d_beta);
d0_gamma=d0*d_gamma_R;
d0_delta=d0*d_delta_R;

/* Inverters times */
d0_time=(float)(0x3E7)*(d0_gamma*0.5);
d1_time=(float)(0x3E7)*(d_alpha_gamma);
d2_time=(float)(0x3E7)*(d_beta_gamma);
d3_time=(float)(0x3E7)*(0.5*(d0_gamma+d0_delta));
d4_time=(float)(0x3E7)*(d_beta_delta);
d5_time=(float)(0x3E7)*(d_alpha_delta);
d6_time=(float)(0x3E7)*(d0_delta*0.5);
```

A3.2.2 SVM for common-mode voltage reduction

```
V_ref=220*f_ref/f_base; //output reference voltage
w=two_pi*f_ref;
m=ksqrt3_2*V_ref/220; //modulation index


/* Reference angle calculation */
theta_i=theta_i+w*Dt;
theta_i=((theta_i>two_pi)?(theta_i-two_pi):theta_i);

/* Sector calculation */
sector_i=(theta_i+pi_3)/pi_3;
sector_i=((sector_i==7)?1:sector_i);

offsetangle_i=(sector_i-1)*pi_3;
theta_ref_i=theta_i-offsetangle_i;

/* Duty cycles */
d1=(d_gamma+d_delta)*m*sinsp(pi_3-theta_ref_i);
d2=(d_gamma+d_delta)*m*sinsp(theta_ref_i);

/* Zero vectors */
vect011=vector_inv[0]; vect012=vector_inv[7];
vect021=vector_inv[7]; vect022=vector_inv[0];

/* Vectors selection depending on the sector */
if (sector_i==1){
    vect11=vector_inv[1]; vect12=vector_inv[6];
    vect21=vector_inv[3]; vect22=vector_inv[4];
    d_alpha=d1; d_beta=d2;
}
else if (sector_i==2){
    vect11=vector_inv[2]; vect12=vector_inv[5];
    vect21=vector_inv[3]; vect22=vector_inv[4];
    d_alpha=d2; d_beta=d1;
}
else if (sector_i==3){
    vect11=vector_inv[2]; vect12=vector_inv[5];
```

```
    vect21=vector_inv[6]; vect22=vector_inv[1];
    d_alpha=d1; d_beta=d2;
}
else if (sector_i==4){
    vect11=vector_inv[4]; vect12=vector_inv[3];
    vect21=vector_inv[6]; vect22=vector_inv[1];
    d_alpha=d2; d_beta=d1;
}
else if (sector_i==5){
    vect11=vector_inv[4]; vect12=vector_inv[3];
    vect21=vector_inv[5]; vect22=vector_inv[2];
    d_alpha=d1; d_beta=d2;
}
else{
    vect11=vector_inv[1]; vect12=vector_inv[6];
    vect21=vector_inv[5]; vect22=vector_inv[2];
    d_alpha=d2; d_beta=d1;
}

/* Combined duty cycles */
d_alpha_gamma=d_alpha*d_gamma_R;
d_alpha_delta=d_alpha*d_delta_R;
d_beta_gamma=d_beta*d_gamma_R;
d_beta_delta=d_beta*d_delta_R;
d0=1-(d_alpha+d_beta);
d0_gamma=d0*d_gamma_R;
d0_delta=d0*d_delta_R;

/* x coefficient calculation */
x=(3*(d0_gamma + d0_delta) - d_alpha_gamma - d_alpha_delta + d_beta_gamma +
d_beta_delta)/(6*(d0_gamma + d0_delta));

/* Inverters times */
d0_time=(float)(0x3E7)*(d0_gamma*aux);
d1_time=(float)(0x3E7)*(d_alpha_gamma);
d2_time=(float)(0x3E7)*(d_beta_gamma);
d3_time=(float)(0x3E7)*((1-aux)*(d0_gamma+d0_delta));
d4_time=(float)(0x3E7)*(d_beta_delta);
d5_time=(float)(0x3E7)*(d_alpha_delta);
d6_time=(float)(0x3E7)*(d0_delta*aux);
```

The loading of inverters times, shown below, is the same independent of the modulation strategy used for the power converter output stages.

```
/* Inverters times loading */
if (d0_time>1){
    *dpr3=vect011|(d0_time);
    *dpr4=vect012|(d0_time);
}
if (d1_time>1){
    *dpr3=vect11|(d1_time);
    *dpr4=vect12|(d1_time);
}
if (d2_time>1){
    *dpr3=vect21|(d2_time);
```

```
    *dpr4=vect22|(d2_time);
}
if (d3_time>1){
    *dpr3=vect021|(d3_time);
    *dpr4=vect022|(d3_time);
}
if (d4_time>1){
    *dpr3=vect21|(d4_time);
    *dpr4=vect22|(d4_time);
}
if (d5_time>1){
    *dpr3=vect11|(d5_time);
    *dpr4=vect12|(d5_time);
}
    *dpr3=vect011|(0x000);
    *dpr4=vect012|(0x000);
}
```

Appendix 4. Measurement boards circuits

The schematic circuits of the boards used to measure voltages and currents and the board used to read the encoder are shown in this Appendix.

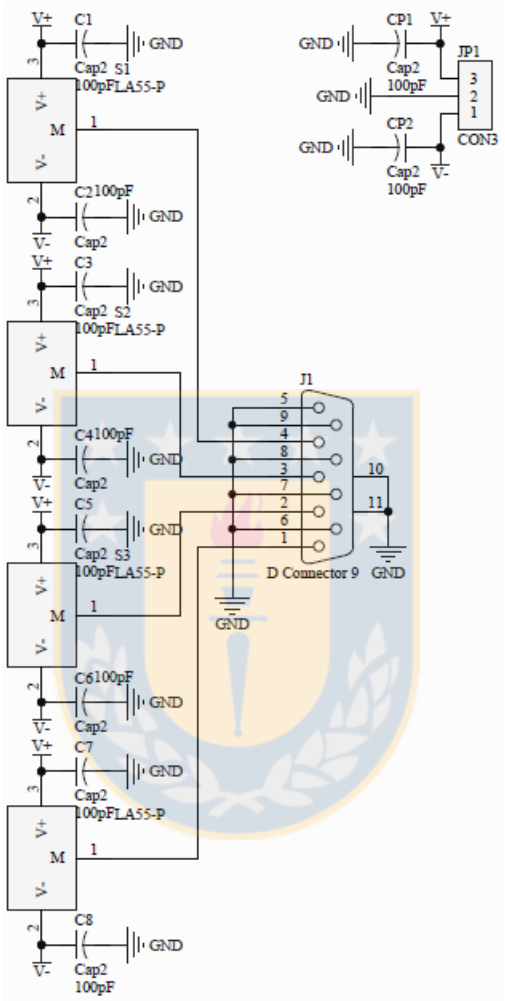


Fig. A4.1. Schematic diagram of the current measurement board

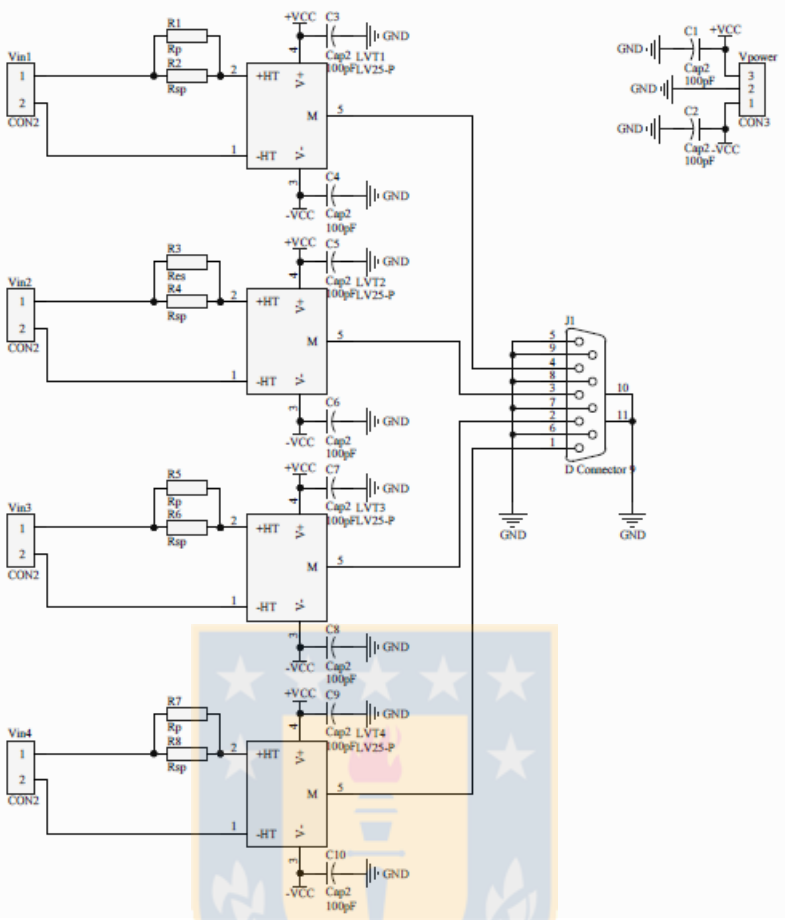


Fig. A4.2. Schematic diagram of the voltage measurement board

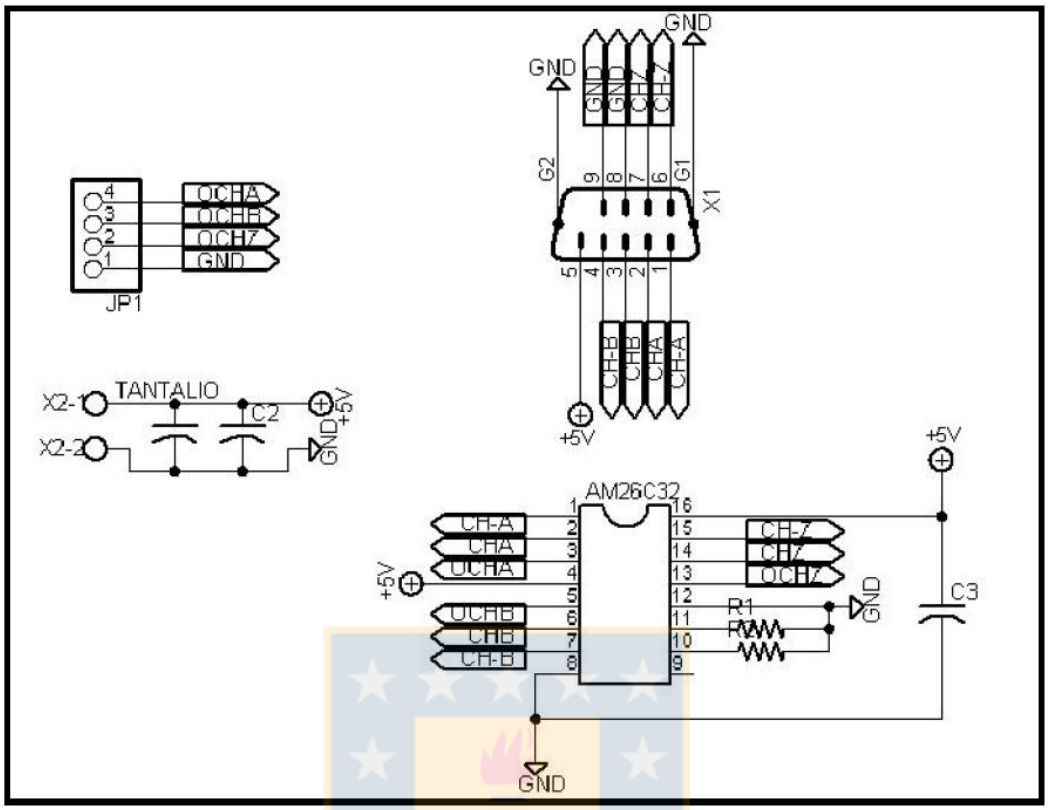


Fig. A4.3. Schematic diagram of the encoder reading board

References

[1] S. Chen, “Bearing current, EMI and soft switching in induction motor drives—A systematic analysis, design and evaluation,” Ph.D. dissertation, Univ. Wisconsin, Madison, 1995.

[2] M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, “Effect of PWM inverters on ac motor bearing currents and shaft voltages,” *IEEE Trans. Ind. Applicat.*, vol. 32, no. 2, pp. 250–259, 1996.

[3] Hedayati, M.H.; Acharya, A.B.; John, V., "Common-Mode Filter Design for PWM Rectifier-Based Motor Drives," *Power Electronics, IEEE Transactions on* , vol.28, no.11, pp.5364,5371, Nov. 2013.

[4] Fang Luo; Dong Dong; Boroyevich, D.; Mattavelli, P.; Shuo Wang, "Improving High-Frequency Performance of an Input Common Mode EMI Filter Using an Impedance-Mismatching Filter," *Power Electronics, IEEE Transactions on* , vol.29, no.10, pp.5111,5115, Oct. 1 2014.

[5] Sujod, M.Z.; Erlich, I., "Harmonics and common mode voltage in a DFIG with two-level and three-level NPC converter using standard PWM techniques," *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE* , vol., no., pp.1650,1655, 10-13 Nov. 2013.

[6] Yang Wang; Panda, D.; Lipo, T.A; Di Pan, "Open-Winding Power Conversion Systems Fed by Half-Controlled Converters," *Power Electronics, IEEE Transactions on* , vol.28, no.5, pp.2427,2436, May 2013.

[7] Wang, Y.; Lipo, T.A; Pan, D., "Robust operation of double-output AC machine drive," *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on* , vol., no., pp.140,144, May 30 2011-June 3 2011.

[8] Kolar, J.W.; Friedli, T.; Rodriguez, J.; Wheeler, P.W., "Review of Three-Phase PWM AC–AC Converter Topologies," *Industrial Electronics, IEEE Transactions on* , vol.58, no.11, pp.4988,5006, Nov. 2011.

[9] Mohapatra, K.K.; Gopakumar, K.; Somasekhar, V.T.; Umanand, L.; , "A harmonic elimination and suppression scheme for an open-end winding induction motor drive," *Industrial Electronics, IEEE Transactions on*, vol.50, no.6, pp. 1187- 1198, Dec. 2003.

[10] George, D.S.; Baiju, M.R.; , "Decoupled random modulation technique for an open-end winding induction motor based 3-level inverter," *Industrial Electronics & Applications, 2009. ISIEA 2009. IEEE Symposium on*, vol.2, no., pp.1022-1027, 4-6 Oct. 2009.

[11] Ramachandrasekhar, K.; Mohan, S.; Srinivas, S.; , "An improved PWM for a dual two-level inverter fed open-end winding induction motor drive," *Electrical Machines (ICEM), 2010 XIX International Conference on* , vol., no., pp.1-6, 6-8 Sept. 2010.

[12] Reddy, B.V.; Somasekhar, V.T.; , "A decoupled SVPWM technique for a dual inverter four-level open-end winding induction motor drive with voltage balancing of Dc-link capacitors," *Power Electronics, Drives and Energy Systems (PEDES) & 2010 Power India, 2010 Joint International Conference on* , vol., no., pp.1-6, 20-23 Dec. 2010.

[13] Sekhar, K.R.; Srinivas, S., "Discontinuous Decoupled PWMs for Reduced Current Ripple in a Dual Two-Level Inverter Fed Open-End Winding Induction Motor Drive," *Power Electronics, IEEE Transactions on* , vol.28, no.5, pp.2493,2502, May 2013.

[14] Srinivas, S.; Ramachandra Sekhar, K., "Theoretical and Experimental Analysis for Current in a Dual-Inverter-Fed Open-End Winding Induction Motor Drive With Reduced Switching PWM," *Industrial Electronics, IEEE Transactions on* , vol.60, no.10, pp.4318,4328, Oct. 2013.

[15] Kalaiselvi, J.; Srinivas, S., "Passive common mode filter for reducing shaft voltage, ground current, bearing current in dual two level inverter fed open end winding induction motor," *Optimization of Electrical and Electronic Equipment (OPTIM), 2014 International Conference on* , vol., no., pp.595,600, 22-24 May 2014.

[16] Kalaiselvi, J.; Srinivas, S., "Bearing Currents and Shaft Voltage Reduction in Dual-Inverter-Fed Open-End Winding Induction Motor With Reduced CMV PWM Methods," *Industrial Electronics, IEEE Transactions on* , vol.62, no.1, pp.144,152, Jan. 2015.

[17] Zhu, B.; Prasanna, U.R.; Rajashekara, K.; Kubo, H., "Comparative study of PWM strategies for three-phase open-end winding induction motor drives," *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International* , vol., no., pp.395,402, 18-21 May 2014.

[18] Bodo, N.; Levi, E.; Jones, M., "Investigation of Carrier-Based PWM Techniques for a Five-Phase Open-End Winding Drive Topology," *Industrial Electronics, IEEE Transactions on* , vol.60, no.5, pp.2054,2065, May 2013.

[19] Bodo, N.; Levi, E.; Jones, M., "Enhanced decoupling PWM methods for five-phase open-end winding drives," *Electrical Machines (ICEM), 2012 XXth International Conference on* , vol., no., pp.939,945, 2-5 Sept. 2012.

[20] Patkar, F.; Levi, E.; Jones, M., "A six-phase multilevel space vector PWM algorithm for a dual-inverter supplied drive," *Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on* , vol., no., pp.1,5, 27-29 March 2012.

[21] Bodo, N.; Jones, M.; Levi, E., "Multi-level space-vector PWM algorithm for seven-phase open-end winding drives," *Industrial Electronics (ISIE), 2011 IEEE International Symposium on* , vol., no., pp.1881,1886, 27-30 June 2011.

[22] V.T. Somasekhar, K. Gopakumar, E.G. Shivakumar, S.K. Sinha, “A space vector modulation scheme for a dual two level inverter fed open end winding induction motor drive for the elimination of zero sequence currents”, *European Power Electronic and Drives Journal*, Vol.12, no. 2, March 2002.

[23] Oleschuk, V.; Sizov, A.; Bose, B.K.; Stankovic, A.M., "Phase-Shift-Based Synchronous Modulation of Dual Inverters for an Open-End Winding Motor Drive with Elimination of Zero Sequence Currents," *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on* , vol.1, no., pp.325,330, 16-18 Jan. 2006.

[24] Somasekhar, V.T.; Srinivas, S.; Prakash Reddy, B.; Nagarjuna Reddy, C.; Sivakumar, K.; , "Pulse width-modulated switching strategy for the dynamic balancing of zero-sequence current for a dual-inverter fed open-end winding induction motor drive," *Electric Power Applications, IET* , vol.1, no.4, pp.591-600, July 2007.

[25] Somasekhar, V.T.; Srinivas, S.; Kumar, K.K., "Effect of Zero-Vector Placement in a Dual-Inverter Fed Open-End Winding Induction-Motor Drive With a Decoupled Space-Vector PWM Strategy," *Industrial Electronics, IEEE Transactions on* , vol.55, no.6, pp.2497,2505, June 2008.

[26] Senicar, F.; Junge, C.; Gruber, S.; Soter, S., "Zero sequence current elimination for dual-inverter fed machines with open-end windings," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.853,856, 7-10 Nov. 2010.

[27] Srinivasan, P.; Reddy, B.V.; Somasekhar, V.T.; , "PWM switching strategy for the elimination of common mode voltage of a two-level inverter drive with an open-end winding induction motor configuration," *Power Electronics, Drives and Energy Systems (PEDES) & 2010 Power India, 2010 Joint International Conference on*, vol., no., pp.1-6, 20-23 Dec. 2010.

[28] Somani, A.; Gupta, R.K.; Mohapatra, K.K.; Basu, K.; Mohan, N.; , "Modulation strategies for direct-link drive for open-end winding AC machines," *Electric Machines and Drives Conference, 2009. IEMDC '09. IEEE International*, vol., no., pp.1863-1868, 3-6 May 2009.

[29] Somani, A.; Gupta, R.K.; Mohapatra, K.K.; Mohan, N.; , "A minimum-switch direct-link drive with common-mode voltage suppression and active filtering for open-end winding AC machines," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, vol., no., pp.2889-2893, 15-19 June 2008.

[30] Somasekhar, V.T.; Gopakumar, K.; Pittet, A.; Ranganathan, V.T., "PWM inverter switching strategy for a dual two-level inverter fed open-end winding induction motor drive with a switched neutral," *Electric Power Applications, IEE Proceedings* - , vol.149, no.2, pp.152,160, Mar 2002.

[31] Somasekhar, V.T.; Gopakumar, K.; Baiju, M.R., "Dual two-level inverter scheme for an open-end winding induction motor drive with a single DC power supply and improved DC bus utilisation," *Electric Power Applications, IEE Proceedings* - , vol.151, no.2, pp.230,238, Mar 2004.

[32] Bodo, N.; Jones, M.; Levi, E., "PWM techniques for an open-end winding fivephase drive with a single DC source supply," *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.3641,3646, 25-28 Oct. 2012.

[33] Bodo, N.; Jones, M.; Levi, E.; Iqbal, A., "PWM techniques for an open-end winding seven-phase drive with a single DC source supply," *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE* , vol., no., pp.5209,5214, 10-13 Nov. 2013.

[34] Rajeevan, P.P.; Abu-Rub, H.; Iqbal, A.; Gopakumar, K., "Common mode voltage elimination scheme for dual-inverter fed five phase AC drives with open-end stator windings," *Industrial Technology (ICIT), 2013 IEEE International Conference on* , vol., no., pp.1680,1685, 25-28 Feb. 2013.

[35] Bodo, N.; Jones, M.; Levi, E., "A Space Vector PWM With Common-Mode Voltage Elimination for Open-End Winding Five-Phase Drives With a Single DC Supply," *Industrial Electronics, IEEE Transactions on* , vol.61, no.5, pp.2197,2207, May 2014.

[36] Kanchan, R.S.; Tekwani, P.N.; Gopakumar, K., "Three-Level Inverter Scheme With Common Mode Voltage Elimination and DC Link Capacitor Voltage Balancing for an Open-End Winding Induction Motor Drive," *Power Electronics, IEEE Transactions on* , vol.21, no.6, pp.1676,1683, Nov. 2006.

[37] Figarado, S.; Gopakumar, K.; Mondal, G.; Sivakumar, K.; Dinesh, N.S., "Three-Level Inverter Fed Open- end Winding IM Drive with Common Mode Voltage Elimination and Reduced Power Device Count," *Industrial*

Electronics Society, 2007. IECON 2007. 33rd Annual Conference of the IEEE , vol., no., pp.1238,1243, 5-8 Nov. 2007.

[38] Figarado, S.; Bhattacharya, T.; Mondal, G.; Gopakumar, K., "Three-level inverter scheme with reduced power device count for an induction motor drive with common-mode voltage elimination," *Power Electronics, IET* , vol.1, no.1, pp.84,92, March 2008.

[39] Kanchan, R.S.; Tekwani, P.N.; Baiju, M.R.; Gopakumar, K.; Pittet, A., "Three-level inverter configuration with common-mode voltage elimination for induction motor drive," *Electric Power Applications, IEE Proceedings - *, vol.152, no.2, pp.261,270, 4 March 2005.

[40] Baiju, M.R.; Gopakumar, K.; Mohapatra, K.K.; Somasekhar, V.T.; Umanand, L., "Five-level inverter voltage-space phasor generation for an open-end winding induction motor drive," *Electric Power Applications, IEE Proceedings - *, vol.150, no.5, pp.531,538, 9 Sept. 2003.

[41] Mondal, G.; Gopakumar, K.; Tekwani, P.N.; Levi, E., "A Reduced-Switch-Count Five-Level Inverter With Common-Mode Voltage Elimination for an Open-End Winding Induction Motor Drive," *Industrial Electronics, IEEE Transactions on* , vol.54, no.4, pp.2344,2351, Aug. 2007.

[42] Figarado, S.; Sivakumar, K.; Ramchand, R.; Das, A.; Patel, C.; Gopakumar, K., "Five-level inverter scheme for an open-end winding induction machine with less number of switches," *Power Electronics, IET* , vol.3, no.4, pp.637,647, July 2010.

[43] Chandra Sekhar, K.; Tulasi Ram Das, G., "Five-level SPWM Inverter for an Induction Motor with Open-end Windings," *Power and Energy Conference, 2006. PECon '06. IEEE International* , vol., no., pp.342,347, 28-29 Nov. 2006.

[44] Rajeevan, P.P.; Sivakumar, K.; Gopakumar, K.; Patel, C.; Abu-Rub, H., "A Nine-Level Inverter Topology for Medium-Voltage Induction Motor Drive With Open-End Stator Winding," *Industrial Electronics, IEEE Transactions on* , vol.60, no.9, pp.3627,3636, Sept. 2013.

[45] Mathew, J.; Rajeevan, P.P.; Mathew, K.; Azeez, N.A.; Gopakumar, K., "A Multilevel Inverter Scheme With Dodecagonal Voltage Space Vectors Based on Flying Capacitor Topology for Induction Motor Drives," *Power Electronics, IEEE Transactions on* , vol.28, no.1, pp.516,525, Jan. 2013.

[46] Rao, G.S.; Sekhar, K.C., "An eleven-level inverter system for dual-fed induction motor drive," *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on* , vol., no., pp.1,6, 16-19 Dec. 2012.

[47] Chandra Sekhar, K.; Das, G.T.R., "A Nine-Level Inverter System for an Open-End Winding Induction Motor Drive," *Industrial Electronics and Applications, 2006 1ST IEEE Conference on* , vol., no., pp.1,6, 24-26 May 2006.

[48] Sudharshan Kaarthik, R.; Gopakumar, K.; Mathew, J.; Undeland, T., "An open-end winding IM drive with multilevel 12-sided polygonal vectors with symmetric triangles," *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on* , vol., no., pp.1,9, 26-28 Aug. 2014.

[49] Mondal, G.; Sivakumar, K.; Ramchand, R.; Gopakumar, K.; Levi, E., "A Dual Seven-Level Inverter Supply for an Open-End Winding Induction Motor Drive," *Industrial Electronics, IEEE Transactions on* , vol.56, no.5, pp.1665,1673, May 2009.

[50] Zhu, B.; Jia, Y.; Prasanna, U.R.; Rajashekara, K.; Kubo, H., "An input switched multilevel inverter for open-end winding induction motor drive," *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International* , vol., no., pp.1594,1600, 18-21 May 2014.

[51] Nayli, A.; Guizani, S.; Ben Ammar, F., "Open-end winding induction machine supplied by two flying capacitor multilevel inverters," *Electrical Engineering and Software Applications (ICEESA), 2013 International Conference on* , vol., no., pp.1,6, 21-23 March 2013.

[52] Chandra Sekhar, K.; Das, G.T.R., "An Eight-level Inverter System for an Induction Motor with Open-end Windings," *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on* , vol.1, no., pp.219,223, 0-0 0.

[53] Wheeler, P.W.; Rodriguez, J.; Clare, J.C.; Empringham, L.; Weinstein, A, "Matrix converters: a technology review," *Industrial Electronics, IEEE Transactions on* , vol.49, no.2, pp.276,288, Apr 2002.

[54] Gupta, R.K.; Somani, A.; Mohapatra, K.K.; Mohan, N., "Space vector PWM for a direct matrix converter based open-end winding ac drives with enhanced capabilities," *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE* , vol., no., pp.901,908, 21-25 Feb. 2010.

[55] Gupta, R.K.; Mohapatra, K.K.; Somani, A.; Mohan, N., "Direct-Matrix-Converter-Based Drive for a Three-Phase Open-End-Winding AC Machine With Advanced Features," *Industrial Electronics, IEEE Transactions on* , vol.57, no.12, pp.4032,4042, Dec. 2010.

[56] Mohapatra, K.K.; Mohan, N., "Open-End Winding Induction Motor Driven With Matrix Converter For Common-Mode Elimination," *Power Electronics, Drives and Energy Systems, 2006. PEDES '06. International Conference on* , vol., no., pp.1,6, 12-15 Dec. 2006.

[57] Rzasa, J., "Research on dual matrix converter feeding an open-end-winding load controlled with the use of rotating space vectors," *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE* , vol., no., pp.4919,4924, 10-13 Nov. 2013.

[58] Rzasa, J.; Garus, G., "Research on dual matrix converter feeding an open-end-winding load controlled with the use of rotating space vectors," *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE* , vol., no., pp.4925,4930, 10-13 Nov. 2013.

[59] Iqbal, A.; Alammari, R.; Abu-Rub, H.; Ahmed, S.M., "PWM scheme for dual matrix converters based five-phase open-end winding drive," *Industrial Technology (ICIT), 2013 IEEE International Conference on* , vol., no., pp.1686,1690, 25-28 Feb. 2013.

[60] Ahmed, S.M.; Abu-Rub, H.; Salam, Z., "Space vector control of dual matrix converters based five-phase open-end winding drive," *Energy Conversion (CENCON), 2014 IEEE Conference on* , vol., no., pp.348,353, 13-14 Oct. 2014.

[61] Ahmed, S.M.; Abu-Rub, H.; Salam, Z.; Iqbal, A., "Dual matrix converters based seven-phase open-end winding drive," *Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on* , vol., no., pp.2105,2110, 1-4 June 2014.

[62] Ahmed, S.M.; Salam, Z.; Abu-Rub, H., "Common-mode voltage elimination in a three-to-seven phase dual matrix converter feeding a seven phase open-end induction motor drive," *Energy Conversion (CENCON), 2014 IEEE Conference on* , vol., no., pp.207,212, 13-14 Oct. 2014.

[63] Tewari, S.; Gupta, R.K.; Mohan, N., "Three-level indirect matrix converter based open-end winding AC machine drive," *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.1636,1641, 7-10 Nov. 2011.

[64] Rashid, M. Power Electronics: *Circuits, Devices, and Applications.* 3ed. 2003. ISBN: 0131011405.

[65] C. Klumpner, F. Blaabjerg, Modulation method for a multiple drive system based on a two-stage direct power conversion topology with reduced input current ripple, IEEE Trans. on Power Electron. 20, (2005) 922- 929.

[66] J.W. Kolar, F. Schafmeister, Novel modulation schemes minimizing the switching losses of sparse matrix converters, The 29th Annual Conf. of the IEEE Ind. Electron. Soc. (2003) IECON '03, 2085 – 2090.

[67] Mohan, N., Undeland, T., Robbins, W. Power Electronics: *Converters, Applications, and Design*.3ed. 2002. ISBN: 0471226939.

[68] Costa, L.L.H.; Serni, P.J.A.; Marafao, F.P., "An analysis of Generalized Symmetrical Components in non sinusoidal three phase systems," *Power Electronics Conference (COBEP), 2011 Brazilian* , vol., no., pp.502,507, 11-15 Sept. 2011.

[69] Ma Hongfei; Xu Dianguo; Miao Lijie, "Suppression techniques of common-mode voltage generated by voltage source PWM inverter," *Power Electronics and Motion Control Conference, 2004. IPEMC 2004. The 4th International* , vol.3, no., pp.1533,1538 Vol.3, 14-16 Aug. 2004.

[70] Shaotang Chen; Lipo, T.A.; Fitzgerald, D., "Modeling of motor bearing currents in PWM inverter drives," *Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95., Conference Record of the 1995 IEEE* , vol.1, no., pp.388,393 vol.1, 8-12 Oct 1995.

[71] Pena, R.; Cardenas, R.; Reyes, E.; Clare, J.; Wheeler, P., "Control of a Doubly Fed Induction Generator via an Indirect Matrix Converter With Changing DC Voltage," *Industrial Electronics, IEEE Transactions on* , vol.58, no.10, pp.4664,4674, Oct. 2011.

[72] Hava, A.M.; Kerkman, R.J.; Lipo, T.A., "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *Power Electronics, IEEE Transactions on* , vol.14, no.1, pp.49,61, Jan 1999.

[73] Riedemann, J.; Peña, R.; Cárdenas, R., "Estrategias de modulación para el control de un motor de inducción de terminales abiertos vía convertidor matricial indirecto de dos salidas", *Congreso de la asociación chilena de control automático (ACCA) 2012*.

[74] Riedemann, Javier; Pena, Ruben; Cardenas, Roberto; Clare, Jon; Wheeler, Pat; Rivera, Marco, "Switching strategies for an indirect matrix converter fed open-end load," *Industrial Electronics (ISIE), 2013 IEEE International Symposium on* , vol., no., pp.1,6, 28-31 May 2013.

[75] Riedemann, J.; Pena, R.; Cardenas, R.; Clare, J.; Wheeler, P.; Rivera, M., "Common mode voltage and zero sequence current reduction in an open-end load fed by a two output indirect matrix converter," *Power Electronics and Applications (EPE), 2013 15th European Conference on* , vol., no., pp.1,9, 2-6 Sept. 2013.

[76] Riedemann, J.; Pena, R.; Cardenas, R.; Rivera, M.; Blasco-Gimenez, R.; Clare, J.; Wheeler, P., "Control of an open-end winding induction machine via a two-output indirect matrix converter," *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE* , vol., no., pp.1537,1544, 16-20 March 2014.

[77] Riedemann, J.; Peña, R.; Cárdenas, R.; Clare, J.; Wheeler, P.; Blasco-Gimenez, R. “Modulation Strategies for an Open-End Winding Induction Machine fed by a Two-Output Indirect Matrix Converter”, *11th International Conference on Modeling and Simulation of Electric Machines, Converters and Systems (ELECTRIMACS) 2014.*

[78] Riedemann, J.; Pena, R.; Cardenas, R.; Clare, J.; Wheeler, P.; Blasco-Gimenez, R., "Control strategy of a dual-inverter system for an open-end winding induction machine based on indirect matrix converter," *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on* , vol., no., pp.1,8, 26-28 Aug. 2014.

[79] Riedemann Aros, J.; Pena Guinez, R.; Cardenas Dobson, R.; Blasco Gimenez, R.; Clare, J., "Indirect matrix converter modulation strategies for open-end winding induction machine," *Latin America Transactions, IEEE (Revista IEEE America Latina)* , vol.12, no.3, pp.395,401, May 2014.