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Integration of silicon-based MMIC technology for millimeter wave cryogenic receivers

Tesis para optar al grado académico de Doctor en ciencias de la ingeniería con mención en ingeniería eléctrica

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Abstract

This thesis work is framed in the area of astronomical instrumentation, specifically regarding the frequency range of millimeter wave. The demand for efficiency in the astronomical observations of low noise requires the search of new technological alternatives for the development of receivers that observe in a faster manner and with lower associated costs. These receivers work in environments at cryogenic temperature, because this decreases the noise of the electronic devices. The technology used currently to synthesize them is based on indium phosphide (InP) circuits, which has showed the best levels of associated noise. However, it has limited the miniaturization of the receivers. This is why, in this thesis, the integration of silicon-based technology is proposed, which, although has been widely used in commercial applications, it has not yet been used in cryogenic applications in the frequency range of millimeter wave. The progress made in the manufacturing of these circuits has allowed its operation at maximum frequencies higher than 700 GHz, and the high integration of functions in a single chip. Regarding its operation at cryogenic temperatures, up to year 2016, it had been tested up to 25 GHz. In this thesis, the cryogenic characterization of a silicon-germanium (SiGe) low noise amplifier of 60 GHz was presented. In addition, packaging designs are presented for a 75-116 GHz SiGe amplifier. Finally, preliminary designs of silicon-based/InP hybrid solutions in the 180-210 GHz band were presented. These designs were studied for different types of interconnections between both technologies. Silicon-based/InP hybrids solutions take advantage of the characteristics of low noise of the InP and the high integration of the silicon circuits. The obtained results demonstrate a stable operation of this technology at a 20 K temperature in the band of 50 to 70 GHz. At 20 K, the noise performance improved 4.4 times in comparison with the room temperature. The packaging designs showed that the flip-chip is adequate for the ensemble technique of this technology, because it provides a good performance in all the frequency band achieving -7 dB at 115 GHz for the complete packaging system. Hybrid solution with flip-chip interconnection also achieved a good performance with 67 % of the frequency band at 180-210 GHz over 40 dB. The results of this thesis show that it is possible to synthesize integrated millimeter receivers for their implementation in applications such as Earth remote sensing and radio astronomy. In the latter, the hybrid solutions will allow the synthetizing of millimeter cryogenic receivers with hundreds of pixels.

Resumen

Este trabajo está enmarcado en el área de instrumentación astronómica, específicamente en el rango de frecuencias de onda milimétricas. La demanda de eficiencia en las observaciones astronómicas de bajo ruido requiere la búsqueda de nuevas alternativas tecnológicas para el desarrollo de receptores que observen más rápido y con bajos costos asociados. Estos receptores funcionan en ambientes de temperatura criogénica, porque esto disminuye el ruido de los dispositivos electrónicos. La tecnología usada actualmente para sintetizarlos está basada en circuitos de fosfuro de indio (InP), la cual ha demostrado los mejores niveles de ruido asociados. Sin embargo, esta limitando la miniaturización de los receptores. Es por ello que en esta tesis se propone la integración de circuitos basados en silicio, la cual, si bien ha sido ampliamente usada en aplicaciones comerciales, aún no se ha utilizado en aplicaciones criogénicas en el rango de frecuencias de onda milimétricas. Los avances en la fabricación de estos circuitos han hecho posible su operación a frecuencias máximas mayores que 700 GHz y la alta integración de funciones en un mismo chip. Con respecto a su operación a niveles criogénicos, hasta el año 2016 solo se había probado hasta 25 GHz. En esta tesis se presenta la caracterización criogénica de un amplificador de bajo ruido de silicio germanio (SiGe) de 60-GHz. Además, se presentan diseños para empaquetar un amplificador SiGe de 75-116 GHz. Por último, se presentan diseños preliminares híbridos de silicio/InP en la banda de 180-210 GHz. Estos diseños se estudiaron usando distintos tipos de interconexiones entre ambas tecnologías. Las soluciones híbridas de silicio/InP aprovechan las características de bajo ruido de InP y la alta integración de los circuitos de silicio. Los resultados obtenidos demostraron la operación estable de esta tecnología a una temperatura de 20 K en el rango de 50 a 70 GHz. A 20 K su nivel de ruido mejoró 4.4 veces en comparación con temperatura ambiente. Los diseños de empaque mostraron que la técnica de flip-chip es adecuada para el ensamble de esta tecnología, porque proporciona buen rendimiento en toda la banda de frecunacias alcanzando reflexiones de -7 dB a 115 GHz para el sistema completo empaquetado. La solución hibrida con interconexión flip-chip también mostro un buen rendimiento con un 67 % de la banda de 180-210 GHz sobre 40 dB. Los resultados de esta tesis demuestran que es posible la sintetización de receptores milimétricos integrados para aplicaciones como Earth remote sensing y radio-astronomía. En esta última, las soluciones híbridas harán posible la síntesis de receptores criogénicos milimétricos con cientos de pixeles.

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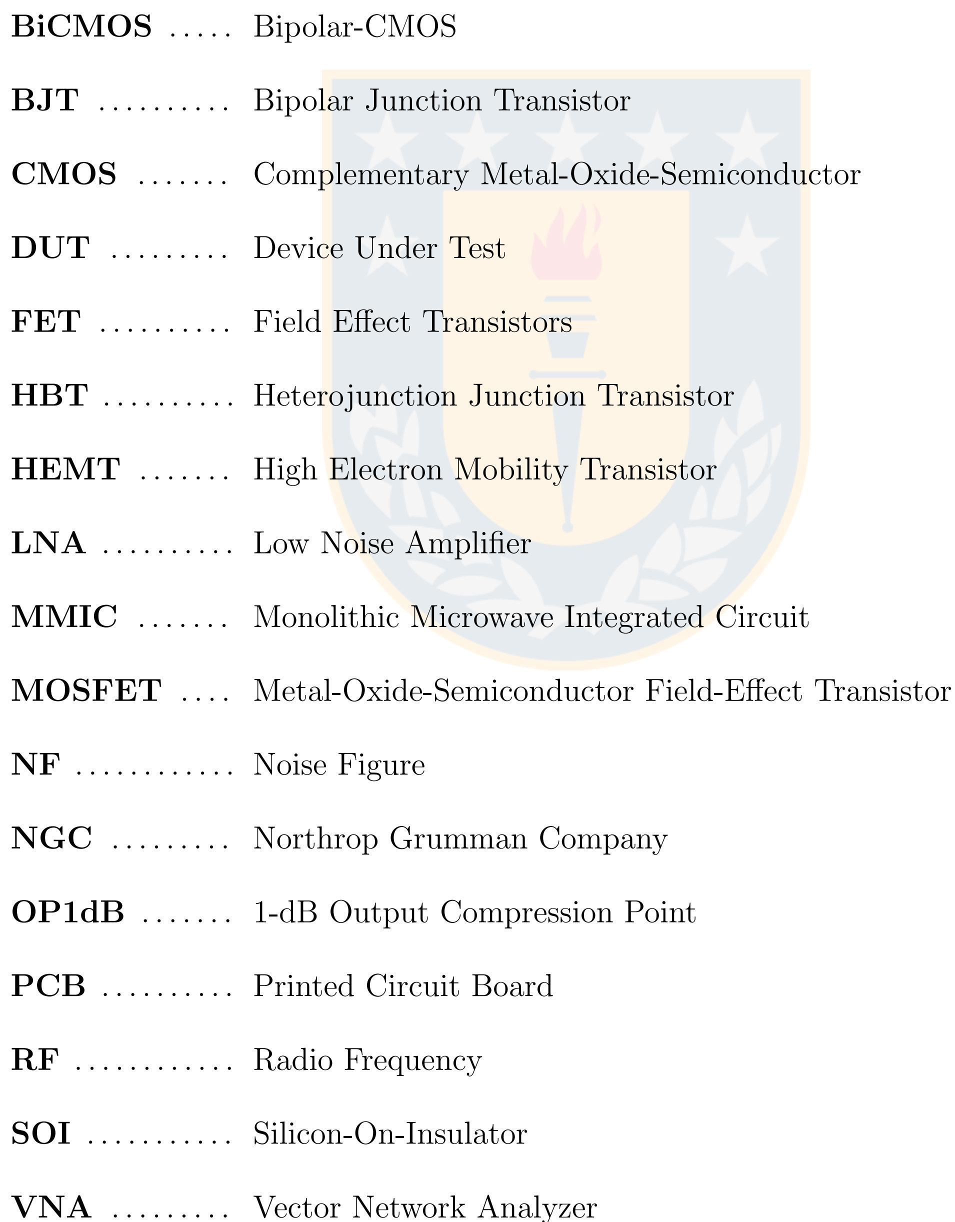
List of Abbreviations



BiCMOS ..... Bipolar-CMOS

BJT .... Bipolar Junction Transistor

CMOS .... Complementary Metal-Oxide-Semiconductor

DUT .... Device Under Test

FET .... Field Effect Transistors

HBT .... Heterojunction Junction Transistor

HEMT .... High Electron Mobility Transistor

LNA .... Low Noise Amplifier

MMIC .... Monolithic Microwave Integrated Circuit

MOSFET .... Metal-Oxide-Semiconductor Field-Effect Transistor

NF .... Noise Figure

NGC .... Northrop Grumman Company

OP1dB .... 1-dB Output Compression Point

PCB .... Printed Circuit Board

RF .... Radio Frequency

SOI .... Silicon-On-Insulator

VNA .... Vector Network Analyzer

1 Introduction

This work is framed in the area of astronomical instrumentation, specifically regarding the development of instruments used to receive waves from space. In this thesis, the waves received are in the millimeter-wave region of the electromagnetic spectrum. This region covers wavelengths from 10 millimeters to 1 millimeter, which correspond to radio frequencies of 30 to 300 GHz. Different parts of the electromagnetic spectrum can be observed, depending on the technology used. For example, Fig. 1.1(a) shows a portion of the sky observed, a galaxy in this case, obtained with imaging instrumentation for the detection of optical waves. In Fig. 1.1(b) the same visible image is observed, this time superimposed over an image of the same portion of the sky but obtained with instrumentation that detects millimeter-waves. As can be noted from the second image made with millimeter-wave instrumentation, it is possible to obtain more information of the same galaxy in this case using this tool. Fig. 1.2 shows a typical receiver that detects millimeter-waves from the sky. This type of receivers are called superheterodyne receivers, they are composed by a horn, followed by a chain of amplifiers to increase the power of the signal. After that, the signal enters to a frequency converter (mixer) that decreases the input frequency for later detection. This lowered frequency signal is conditioned in the stage of intermediate frequencies (IFs) which are generally in the range 2 to 10 GHz. Finally, in the detection stage, the signal can be digitalized and to be processed later.

One of the most important challenges for radio astronomy is how to observe the sky more efficiently, that means, finding the fastest method with the lowest level of associated electronic noise possible. The faster the process of observation, the more it is posible to save on the costs associated. Furthermore, if the observation

FIGURE 1.1: Image of the Hercules Galaxy in the (a) visible wave spectrum and (b) superimposed with an image of the radio-frequency spectrum.

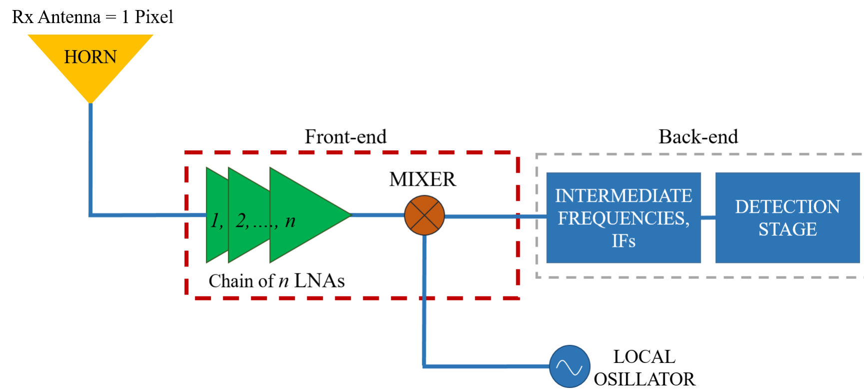


FIGURE 1.2: Typical diagram of a superheterodyne receiver for radio-frequency reception

time of the same portion of the sky is shorter, it is posible to observe more portions of interest in the same amount of time. The mapped velocity and the number of elements of an array have a relationship of linear escalation, [1]:

$$V_{array} = n \times V_{pixel}, \tag{1.1}$$

Where V_{array} is the mapping speed for an array, n is the number of pixels (or horns) in the array and V_{pixel} is the point-source mapping speed for a single horn. In Fig. 1.3 the relationship established by Eq. 1.1 is represented. Image (a) shows a receiver with a single pixel, where 48 receiver pointings are needed to scan sky area “A”. Fig. 1.3(b) shows a receiver of 4 pixels which needs 12 receiver pointings to scan the same portion of sky “A”. The above images demonstrates an increase in sky scan efficiency of 400 %.

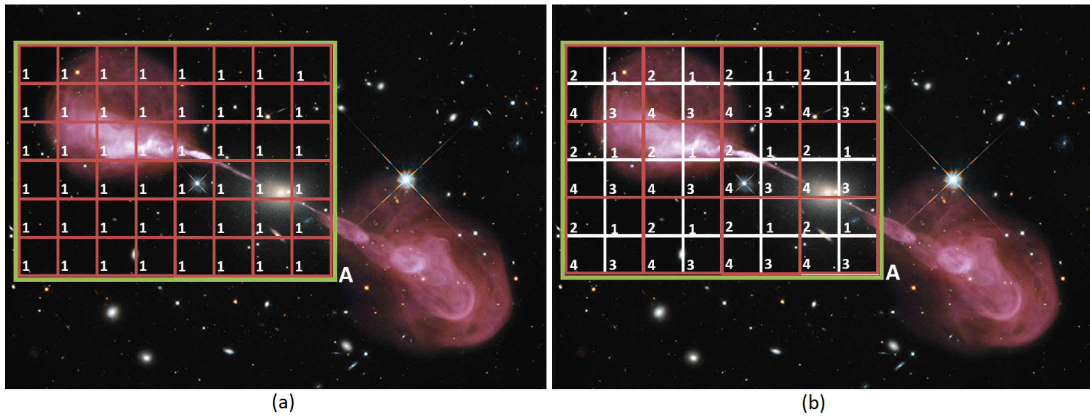


FIGURE 1.3: Scanning process using (a) 1 pixel and (b) 4 pixels

Radio astronomy receivers also require detect even the lowest noise levels, this is because it makes the signal receiver system more sensitive to astronomical objects that emit weaker signals, see Fig. 1.4. This way the instrument has higher sensitivity, hence it is not necessary to observe the same object for a longer time, Eq. 2.3.

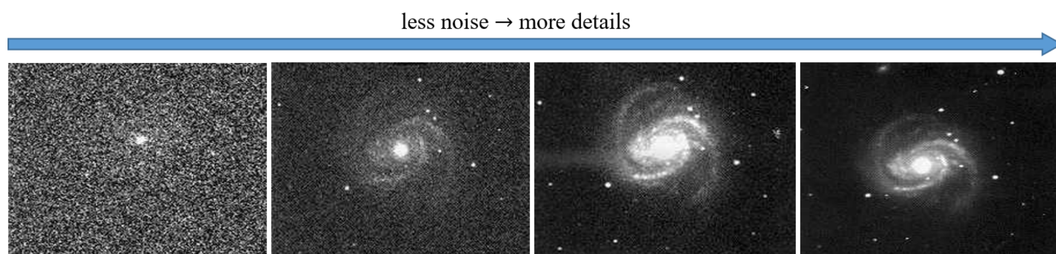


FIGURE 1.4: Explanatory images of electronic noise in astronomical images.

The state of the art is in receiving systems with lower noise and higher number of pixels have been reached of 16 pixels, [2], see Fig. 1.5. The low noise levels are provided by indium phosphide (InP) high electron mobility transistor (HEMT) low noise amplifiers (LNAs). This type of LNAs has demonstrated the lowest noise levels, [3, 4]. However, the integration of several electronic functionalities in a single MMIC has not been possible, due to its large increase in size. Therefore, when having several functions on the front-end of the receiver, it is necessary for the MMICs inside the pixel to be installed one after the other forming a chain. This would translate into having a larger pixel size and consequently a smaller amount of pixels in the focal plane array of the receiver.

The technology proposed for reducing the size of the modules is based on the use of MMICs manufactured with the silicon semiconductor material. This technology

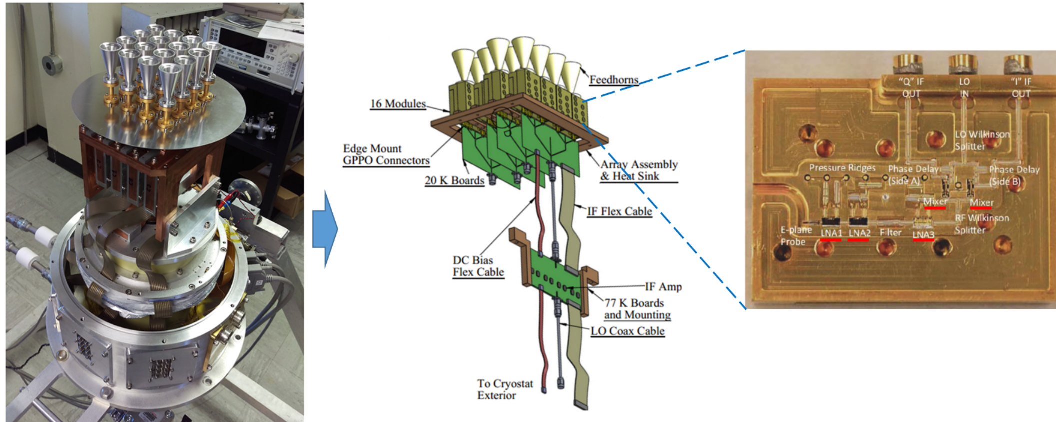


FIGURE 1.5: An 80 to 110 GHz array called Argus, which is installed at the Green Bank telescope, located in West Virginia, USA, [2]. Left: Argus image, which consists of 16 pixels arranged in 4 x 4 matrix form. Middle: Argus diagram, detailing the names of its components. Right: Chain of components inside of an Argus module.

still needs to be tested under the cryogenic environmental conditions in which radio astronomy receivers are used. Along with this, it is necessary to develop cryogenic models of the transistors that are used to design silicon-germanium (SiGe) MMICs. Also, it is necessary to develop packages for the use of these MMICs in real receivers. In this thesis, two of the three works mentioned are addressed: the testing of technology in a cryogenic environment and the design of packaging for SiGe and CMOS MMICs.

1.1 Motivation

The development and integration of silicon-based MMICs will have a high impact on the development of cryogenic receivers, since this technology has demonstrated a high level of integration of electronic functions in the same chip. An example of this integration is shown in Fig. 1.6, where mixing IF amplification and local oscillator stages can be seen in a single chip with an area of 0.575 mm^2. The integration of more functions will reduce the mass and size of the modules for millimeter-wave receivers in radio astronomy and also for radiometric applications and small satellites.

Since silicon-based circuits are not competitive in their noise performance compared to those developed with III-V compounds, especially InP, it is possible to

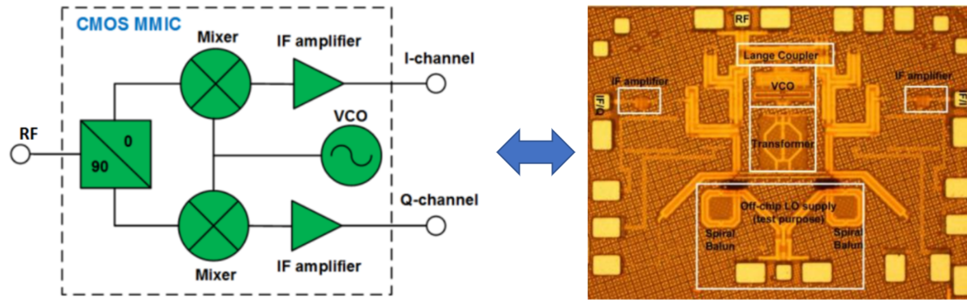


FIGURE 1.6: Micrograph of a CMOS down-converter. The area of the chip is $0.575\ mm^2$, [7].

use a low noise pre-amplification stage using InP technology. This will enable the development of miniaturized modules with low noise figures, low weight and possibly lower power consumption. A diagram of the hybrid solution described is shown in Fig. 1.7.

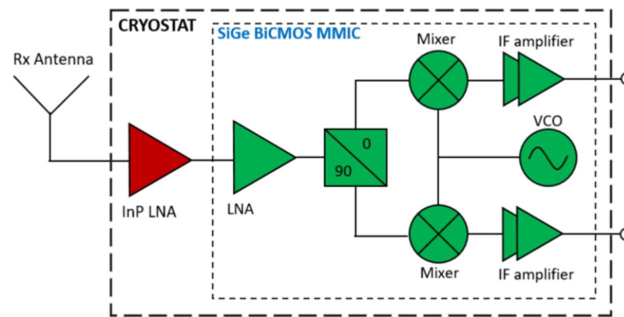


FIGURE 1.7: Hybrid InP/silicon-based solutions for the future low noise and high function integrability microwave cryogenic receivers.

To make progress towards the final development using silicon-based technologies described above, a series of works were carried out in this thesis, which are summarized below:

- Demonstrate the cryogenic operation of a SiGe MMIC LNA at millimeter-wave frequencies of V-band (50-70 GHz) for the first time. Moreover, study whether the cryogenic noise performance is suitable for the use of SiGe amplifier as a second amplification stage for a radio astronomy receiver front-end, where the receiver NF would be determined by the preceding InP HEMT LNA.
- In order to progress in the use of silicon-based MMIC technologies in millimeter-wave frequency cryogenic receivers, it is necessary to design a PCB full integrating the RF and DC circuits for packaging a cryogenic W-Band (75-110

GHz) SiGe BiCMOS LNA. Additionally, RF interconnects between PCB and the LNA must be be studied and their performance must be simulated, in this case both wire-bond or flip-chip interconnects. Both of these are considered for this work, because the wire-bond is the most common interconnects at millimeter-wave frequency, and the flip-chip shows a good performance at these frequencies, [9]. A waveguide block module is necessary to design for the packaging of the PCB with the LNA connected.

- In order to increase the operation frequency range of the packaged silicon-based MMIC technologies and for future low-noise and very integrated receivers, a different interconnects between InP and CMOS MMICs for D-band (140-220 GHz) must be studied. We could call this a hybrid InP/CMOS solution, it is intended to have low noise and several more integrated receiver elements. The latter means there can be more miniaturized elements in the receiver array. InP technology is needed as the first element of the chain of components in order to have very low noise, see Ec. 2.5. After the InP technology, a silicon-based technologies will be connected, similarly to the diagram in Fig. 1.7. The interconnects between both technologies must be studied, using different techniques, as well as different options of substrate materials. The final purpose is to select the best option of interconnect for the next generation of arrays with hundreds of elements.

Finally, this thesis is framed in an international collaborative project for the development of millimeter-wave silicon-based MMIC technology and its use in the next generation of large receiver arrays with hundreds of elements. The collaboration is led by the Finnish research company: VTT Technical Research Centre of Finland, which provided the MilliLab laboratory facilities used for the experiments at cryogenic temperatures of this thesis, as well as the SiGe chips used throughout this research. IHP microelectronics is a research company from Germany, which collaborates with the fabrication of the SiGe MMICs. The third collaborator is the Jet Propulsion Laboratory of the California Institute of Technology from USA, they will provide the InP MMICs.

1.2 Hypothesis

It is possible to develop miniaturized modules in millimeter wave frequency ranges that have a positive impact on the observational efficiency of the reception system, in two different aspects: by reducing the noise temperature of the receiver, and by increasing the possible number of pixels per area unit.

1.3 Objetives

This thesis contributes with advances in the integration of silicon-based MMIC technology for millimeter-wave cryogenic receiving systems. These advances are described in the following main objective and the specific objectives.

1.3.1 Main objective

Demonstrate the cryogenic operation and packaging of the silicon-based MMIC technology for its future integration in millimeter-wave cryogenic receiver systems.

1.3.2 Specific objectives

- Demonstrate the cryogenic operation demonstration of a 60-GHz SiGe low noise amplifier:
  - Carry out stability analysis measuring the output spectrum and its I-V curves at 20 Kelvin and at room temperature.
  - Take noise and gain measurements at 20 Kelvin and at room temperature.
  - Take measurements of the transmission and reflection parameters at 20 Kelvin and at room temperature.
- Present package designs for a W-band silicon-germanium low-noise amplifier:
  - Make a comparison between the wire-bond and flip-chip interconnects using Alumina substrate.

  - Present probe designs using aluminium nitride substrate for implementing flip-chip technique.
  - Present probe designs using megtron 7N substrate for implementing flip-chip technique.

- Present design of 180-210 GHz InP/CMOS hybrid waveguide module interconnects using four types of interconnects:
  - Wire-bond.
  - Flip-chip.
  - Membrane using quartz substrate.
  - Membrane using silicon substrate.

2 Transistor-based receiver performance and characterization

This section presents relevant concepts for the characterization of millimeter-wave systems. For example, parameters associated with the noise in an electronic RF transmitting device and how it can be measured; how the linearity regime of an amplifier can be measured; and how the transmission and reflection parameters of the systems or devices are defined. In addition, the importance of having low noise levels in a receiving system will be observed.

2.1 Receiver performance

2.1.1 Noise temperature

One of the most important parameters in the evaluation of a millimeter wave device or system is its noise temperature. Its importance lies in the fact that its value directly affects how sensitive the system to be used will be. The origin of the concept of noise temperature comes from the thermal agitation of the physical structure of a resistor since it is at a physical temperature above absolute zero (see Fig. 2.1). The thermal agitation induces a zero mean current and nonzero RMS value. This thermal noise is roughly white in spectral terms, and is known by the name Johnson–Nyquist noise in honor of the researchers who studied this phenomenon. Thermal noise produces an average power that can be expressed as [10],

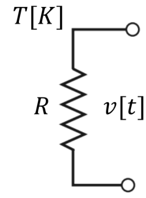


FIGURE 2.1: Resistor R at a physical temperature of *T[K]* that generates a voltage *v[t]*, [10].

$$P = kT\Delta\nu, \tag{2.1}$$

Where k is the Boltzmann constant, $\Delta\nu$ is the bandwidth of the system and T is the physical temperature of the resistor, which is commonly called *noise temperature*. In active components there are two main type of noises, the thermal noise and flicker noise. The thermal noise (Fig. 2.2) is generated by the intrinsic parasitic resistances of the device, and has the same white characteristics as in the case of the resistor. This makes it possible to model thermal noise for an active device using the Eq. 2.1, and in this case the noise temperature (T) is called equivalent noise temperature (T_r). Thermal noise is independent in frequency, while, of course, the noise may be not exactly white up to infinity, we can assume the noise is effectively white into the THz range, [12]. The flicker noise (Fig 2.2) is a phenomenon not widely understood, but has been attributed to imperfections in semiconductor channels and the generation and recombination of charge carriers. However, it is known that flicker noise occurs at low frequencies and that the noise current decreases with frequency exhibiting a 1/f characteristic [13]. Since flicker noise occurs at low frequency, only thermal noise will be taken into account in this work.

2.1.2 Noise Figure

Another way to characterize noise in a microwave device or system is the noise figure. This is a measure of the degradation of the signal-to-noise ratio between the input and output of the device. The signal-to-noise ratio is the ratio between the power of the wanted signal and the power of the unwanted noise, therefore it depends on the power of the signal. By applying noise and a desired signal to the input of a noiseless network, both the noise and the signal will be attenuated or

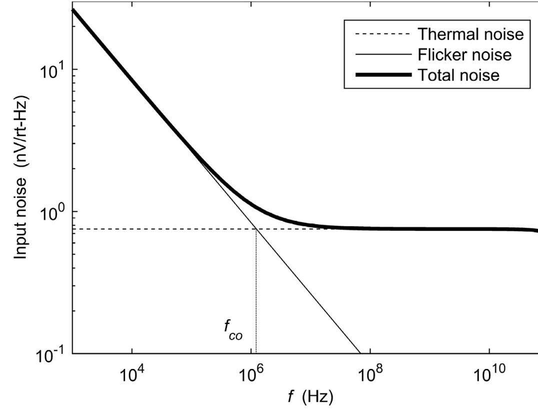


FIGURE 2.2: Power density spectrum of the thermal and flicker noise, [14].

amplified by the same factor, so the signal-to-noise ratio will not change. Meanwhile, if the network is noisy, the output noise power will increase more than the output signal power, thus reducing the output signal-to-noise ratio. The noise figure NF is a measure of this reduction in signal-to-noise ratio and can be calculated as:

$$F = 1 + \frac{T_e}{T_0} \tag{2.2}$$

In dB, it would be: $F = 10log(1 + \frac{T_e}{T_0}) \geq 0$.

2.1.3 Radiometer equation

In order to determine the minimum noise temperature difference that a receiving system (see Fig. 2.3) is able to detect in steady state, we can use the sensitivity equation, and can be defined as,

$$\Delta T_{min} = \frac{K_s T_{sys}}{\sqrt{\Delta\nu \cdot \tau}}, \tag{2.3}$$

Where K_s is a constant related to the architecture of the receiver, τ is the system integration time, $\Delta\nu$ corresponds to the system bandwidth and $T_{sys} = T_A + T_{rx}$, where T_A is the antenna temperature and T_{rx} is the temperature of receiver noise. From this equation, the parameters that directly or indirectly influence sensitivity can be deduced. It is important to mention the direct relationship that T_{rx} has

with sensitivity, for this reason most of the radio astronomy receiving systems are cryogenic. Cryogenic systems help to lower the physical temperature of the receiver electronics and consequently lower the noise temperature associated with the physical temperature.

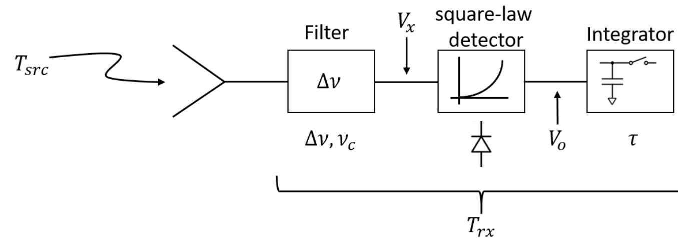


FIGURE 2.3: Simple receiver diagram to exemplify relevant temperatures and variables that define its sensitivity.

2.1.4 Friis equation

The Friis equation is used to calculate the total noise temperature of the cascade system, [15]. Receivers typically require several amplification stages to obtain the desired gain levels. These gain levels can only be obtained by cascading amplifiers (Fig. 2.4), each with a G_i gain. Total gain G is calculated as:

$$G = \prod_{i=1}^{n} G_i \tag{2.4}$$

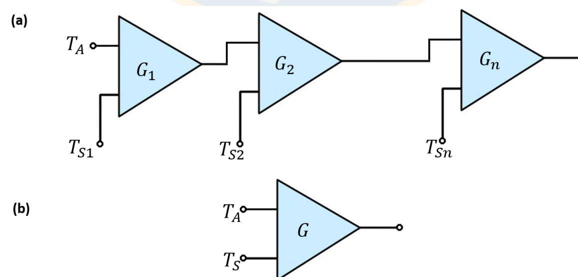


FIGURE 2.4: (a) Cascade amplifiers, the input signals are at the top and the internal noise at the bottom. (b) Resulting diagram of the combined amplifier chain.

The Friis formula takes into account the effect of having amplifiers connected in cascade. So, if we have the amplification stages $1, 2, 3, ..., n$ with their corresponding noise temperatures T_{Si} where $i = 1, 2, 3, ..., n$, the noise temperature (T_S) that takes into account the effect of this chain of amplifiers can be calculated as,

$$T_S = T_{S1} + \frac{1}{G_1}T_{S2} + \frac{1}{G_1G_2}T_{S3} + \cdots + \frac{1}{G_1G_2...G_{n-1}}T_{Sn}, \tag{2.5}$$

Based on Ec. 2.5, when several amplification stages are required, it is recommended to use the amplifier with the best gain and noise performance as the first element.

2.1.5 Measurement of noise temperature: Y-factor method

The most widely used method for measuring noise temperature is the Y-factor method, [10]. With this method it is possible to determine the internal noise in a device under test (DUT), and therefore the noise figure or the effective input noise temperature. To carry out this method, the DUT is connected to one of the two paired loads, which are at different physical temperatures. Then the output power is measured in each case. In Fig 2.5 a diagram of the implementation of the Y-factor method is shown. Y-factor is the ratio of these two powers P_1 and P_2.

$$Y = \frac{P_2}{P_1} \tag{2.6}$$

For instance, assuming that the DUT is an amplifier, the output noise power consists of the noise power generated by the amplifier and the noise power of the source resistor. So we have,

$$P_1 = GkT_1\Delta\nu + GkT_{DUT}\Delta\nu \tag{2.7}$$

$$P_2 = GkT_2\Delta\nu + GkT_{DUT}\Delta\nu \tag{2.8}$$

Then, replacing Ecs. 2.7 and 2.8 in Ec. 2.6, we have:

$$Y = \frac{T_1 + T_{DUT}}{T_2 + T_{DUT}} > 1 \tag{2.9}$$

Using Ec. 2.9 it is possible to obtain the expression for T_{DUT},

$$T_{DUT} = \frac{T_1 - YT_2}{Y - 1} \tag{2.10}$$

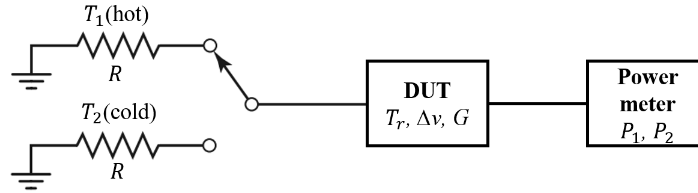


FIGURE 2.5: Diagram of the Y–factor method implementation.

The Y-factor method is the basis for most noise figure measurements, both manual and automated internally in a noise figure analyzer.

2.1.6 Scattering parameters

The scattering parameters or commonly called S-parameters are used for the characterization of n-port networks since these are defined as quotients between incident, reflected and transmitted wave voltages through the n-port network. In Fig. 2.6 we have a two-port network to exemplify the calculated S-parameters:

$$S_{11} = \frac{V_1^-}{V_1^+}, S_{12} = \frac{V_1^-}{V_2^+}, S_{21} = \frac{V_2^-}{V_1^+}, S_{22} = \frac{V_2^-}{V_2^+}, \tag{2.11}$$

They can also be expressed in matrix form:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}$$

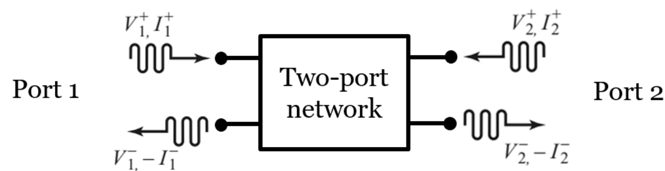


FIGURE 2.6: Two-port network.

In this case, parameter S_{11} is the relationship between the incident wave at port 1 V_1^+ and the wave reflected towards input V_1^-, considering that the other ports end up in matched loads when the S_{11} measurement is being taken. Parameter S_{21} is the relationship between the incident wave on port 1 V_1^+ and the wave transmitted to port 2 V_2^-, considering that the other ports end up in matched loads when the

measurement of S_{21} is being taken. The other parameters can be derived in the same way.

From this example, the calculation of the S-parameters can be generalized and extended to a n-port network, as can be seen in the diagram in Fig. 2.7.

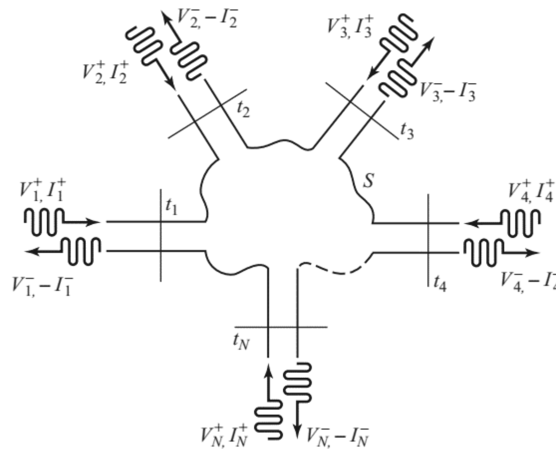


FIGURE 2.7: N–port network, [10]

From this network we can obtain a generalized expression for the calculation of the S-parameters:

$$S_{ij} = \frac{V_i^-}{V_j^+}|_{V_k^+=0} \text{ for } k \neq j \tag{2.12}$$

Turned into words, S_{ij} is found by energizing the port j with a voltage wave V_j^+ and measuring the reflected wave of amplitude V_j^- exiting port i. The incident waves from all ports, except the $j-th$ port, are set to zero, which means that all ports should be terminated at adapted loads to avoid reflections.

- S_{ii} is the reflection coefficient facing port i when all ports are terminated at matched loads.
- S_{ij} is the transmission coefficient from port j to port i when all other ports are terminated at matched loads.

For the measurement of S-parameters, an instrument called vector network analyzer (VNA) is widely used. Fig. 2.8 shows a photograph of one of these instruments. The way a VNA operates is the same way the S-parameters are defined.

FIGURE 2.8: E5080B ENA Vector Network Analyzer, 4-ports, 100 kHz to 53 GHz, [17].

2.1.7 Gain Compression

Gain compression is an effect produced by the high input powers that cause the device to start operating in a nonlinear regime, (Fig 2.9). The device will reach this nonlinear regime because the amount of carriers available in the conduction channel of the transistor is finite, and therefore at some given operating point, the output power will not follow a linear relationship, which should be given by the gain of the device. When an amplifier is characterised, the parameter called 1-dB output compression point (OP1dB) is measured. OP1dB is defined as the output power level at which the gain decreases 1 dB from its constant value (Fig 2.9a). OP1dB is one of the most important specifications for amplifiers, because it indicates the extent to which an amplifier can be considered to operate linearly. In this thesis work, the measurement was carried out, by performing a power sweep of the input, and then performing a power sweep of the output using a power meter. After that, the device gain is calculated assessing the data and verifying that the point in which the gain decreased 1dB. The value of the output power of the amplifier being measured was registered at that point. In case there is an instrument that is able to generate the gain graphic versus power, a simpler way of measuring this parameter is shown in [16]. It proposes measuring the OP1dB directly from the display using the normalized gain parameter for the performed power sweep. The flat part of the trace in Fig. 2.9b is the linear regime, and the curved part on the right side corresponds to the compression caused by higher input power. As shown in Fig 2.9b, the 1 dB compression point of the amplifier under test is 12.3 dBm, at a continuous wave frequency of 902.7 MHz, [16].

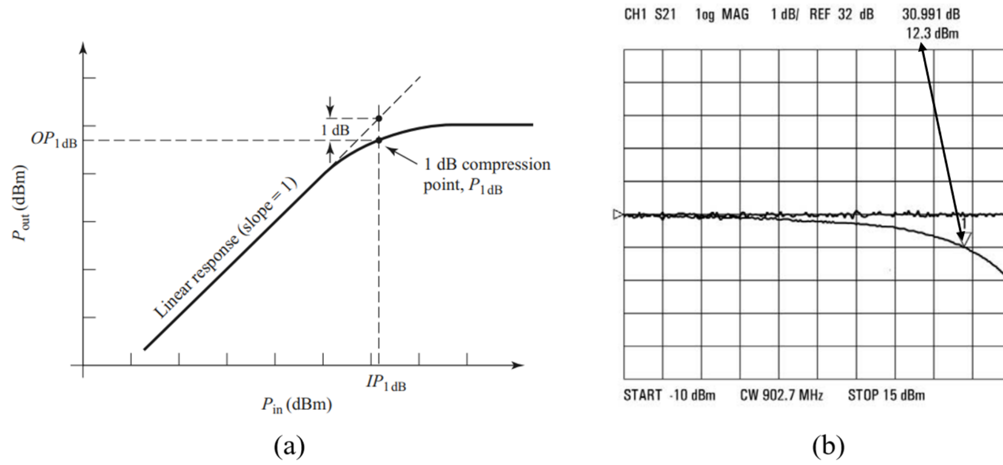


FIGURE 2.9: (a) Definition of the 1-dB output compression point for a nonlinear amplifier, [10]. (b) Measurement of 1-dB output compression point: input power resulting in 1 dB drop in gain, [16].

2.2 Transistor performance and relevant parameters

In order to make of this thesis a more fluent reading from now on, the g_m and β parameters for the bipolar junction transistors (BJTs), and the g_m parameters for field-effect transistors (FETs) are reviewed in this section.

2.2.1 Transconductance g_m and current gain β for transistor

2.2.1.1 Common-emitter current gain, β, for BJTs

The common-emitter current gain is a constant of the transistor specifically, and it is used to express the base current (i_B) as a fraction of the collector current (i_C):

$$i_B = \frac{i_C}{\beta} \tag{2.13}$$

β can be obtained as:

$$\beta = 1/\left(\frac{D_p}{D_n}\frac{N_A}{N_D}\frac{W}{L_p} + \frac{1}{2}\frac{W^2}{D_n \tau_b}\right) \tag{2.14}$$

Where D_p is the difusivity of the emitter gaps, D_n is the electronic difusivity of the base, L_p is the diffusion length of the emitter gaps, N_A is the concentration of contamination of the base, N_D is the concentration of contamination of the emitter, τ_b represents the minority carrier lifetime (is defined as the average time it takes for a minority carrier to recombine with a majority hole of the base), and W effective width of the base. The Eq. 2.14 indicates that in order to obtain a high β (which is highly a desirable gain parameter to have), the base must be thin (small W)and slightly contaminated, and the emitter must be heavily contaminated (small N_A/N_D).

2.2.1.2 Transconductance g_m for BJTs

The transconductance g_m is only determined for the approximation of the small signal of a transistor, and it starts making sense when the transistor is used as an amplifier. Then, if a v_{be} is employed, as shown in Fig. 2.10, the total instantaneous voltage v_{BE} between the emitter and the base turns into:

$$v_{BE} = V_{BE} + v_{be}, \tag{2.15}$$

Where V_{BE} is the polarization voltage between the emitter and the base. That said, assuming that $v_{be} \ll V_T$, it is possible to make an approximation known as small signal. According to this approximation, the current can be expressed as, [18]:

$$i_C = I_C + \frac{I_C}{V_T} v_{be} \tag{2.16}$$

Thus, the collector current consists of the I_C value of DC polarization, and of a i_c signal component:

$$i_c = \frac{I_C}{V_T} v_{be}, \tag{2.17}$$

Where V_T corresponds to the thermal voltage[1]. Eq. 2.17 shows the relation of the signal collector current with the corresponding signal voltage between the base and the emitter. It can be expressed as:

$$i_c = g_m v_{be}, \tag{2.18}$$

where g_m is the transconductance of the bipolar transistor, and is expressed as:

$$g_m = \frac{I_C}{V_T}, \tag{2.19}$$

This reveals that g_m is directly proportional to the polarization current of the collector, I_C. There is a graphic interpretation of g_m in Fig. 2.10. It shows that g_m equals the slope of the curve characteristic i_C–v_{BE} when the current $i_C = I_C$ (in other words, to the polarization point, Q).

$$g_m = \left. \frac{\partial i_C}{\partial v_{BE}} \right|_{i_c = I_C} \tag{2.20}$$

Therefore, for the small signals ($v_{be} \ll V_T$), the transistor behaves as a current source controlled by voltage, where the transconductance of the controlled source is g_m.

[1]Thermal voltage, V_T, is produced due to the thermal agitation of electrons in a medium (in this case in p-n junction) with a temperature greater than absolute zero. As the temperature increases, the electrons begin to receive energy proportional to the temperature, where this constant of proportionality is Boltzmann's constant, k. Therefore, the voltage corresponding to this energy is the thermal voltage, and is calculated as kT/q, where T is the absolute temperature of the p-n junction and q is the magnitude of charge of an electron.

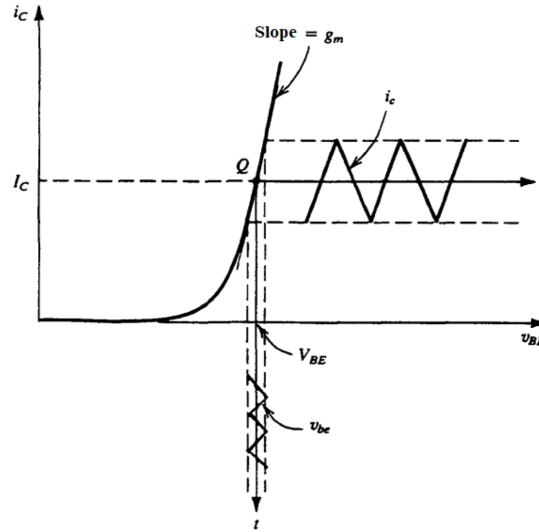


FIGURE 2.10: Linear operation of bipolar transistor under small signal conditions: a small signal v_{be} of triangular wave overlaps on the DC voltage V_{BE}. This gives rise to an i_c current of signal in the collector, which is also of a triangular wave and overlaped on the DC current I_C. $i_c = g_m v_{be}$, where g_m is the slope of the curve i_C–v_{BE} in the Q polarization point, [18].

2.2.1.3 Transconductance g_m for FETs

In these type of transistors the β is not defined, because there is no current flowing from the gate to the drain, as it happens with the bipolar transistor, in case they were considered drain-collector and gate-base analogous. In the FET, the transconductance (g_m) is very important in the characterization of the device, this parameter is defined bellow for one of the most used FET, the MOSFET, Fig. 2.11a.

The transconductance g_m is a parameter defined for the transistor in an amplifier mode, in other words, it works in the saturation region ($V_D > V_{GS} - V_t$). In addition, it is defined for the small signal condition to avoid the non linearity of the transistor. Before showing the development of the expression of the transconductance, an expression that is useful for analyzing the transconductance later on is the polarization current of the DC drain I_D. To find it, the signal, required to be amplified v_{gs}, must be set to zero, and the MOSFET must reach a point in the saturation region. In this point I_D will be:

$$I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2 \tag{2.21}$$

Where W is the width of the network and L is the length of the network, see Fig. 2.11a and V_t is the threshold voltage[2]. k'_n is equal to a $\mu_n C_{ox}$ constant, which is determined by the technology of the process used to manufacture the MOS transistor. This is known as a process transconductance parameter, because it determines the transconductance of the MOSFET and it is measured in A/V^2.

To start the development of the transconductance, the signal, required to be amplified v_{gs}, is considered to be superimposed on V_{GS}, polarization voltage between the gate and the source. The total instanteneous voltage of gate to drain will be, [18]:

$$v_{GS} = V_{GS} + v_{gs} \tag{2.22}$$

Where by considering the small signal condition ($v_{gs} \ll 2(V_{GS} - V_t)$, i_C is expressed as:

$$i_D \cong I_D + i_d \tag{2.23}$$

Where I_D is DC polarization of the drain and i_d is the signal component:

$$i_d = k'_n \frac{W}{L}(V_{GS} - V_t)v_{gs} \tag{2.24}$$

The parameters that presents the relation of i_d and v_{gs} is the g_m transconductance of the MOSFET:

$$g_m \equiv \frac{i_d}{v_{gs}} = k'_n \frac{W}{L}(V_{GS} - V_t) \tag{2.25}$$

In Fig. 2.11b, the graphic interpretation of the MOSFET small signal operation is shown. In these figures, it is possible to notice that g_m is equal to the slope of the curve charcteristic i_D–v_{GS} on the polarization point, Q:

[2]Threshold voltage, V_t, is the gate bias beyond flat-band just starting to induce an inversion charge sheet and is given by the sum of voltages across the semiconductor and the oxide layer, [19].

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}} \tag{2.26}$$

Esta ecuacion es la definicion formal para g_m, [18]. A partir de la Eq. 2.25 es posible obervar que g_m es proporcional al parametro de transconductancia del proceso $k'_n = \mu_n C_{ox}$ y a la razon W/L del transistor. Esto ultimo indica que para obtener una transconductancia relativamente alta, el dispositivo debe ser corto y ancho. g_m tambien es proporcional al voltaje eficaz, $V_{GS} - V_t$, que es la cantidad en la que el voltaje de polarizacion V_{GS} excede al voltaje de umbral V_t. Cabe mensionar, que aumentar g_m polarizando el dispositivo a un V_{GS} mas alto, tiene la desventaja de reducir la oscilacion de seal de voltaje permisible en el drain, [18].

Another expression that is useful for g_m, can be obtained by replacing $(V_{GS} - V_t)$ with $\sqrt{\frac{2I_D}{k'_n(W/L)}}$ (from Eq. 2.21)in Eq. 2.25:

$$g_m = \sqrt{2k'_n}\sqrt{W/L}\sqrt{I_D} \tag{2.27}$$

This expression shows that for a given MOSFET, g_m is porportional to the square root of the polarization current, g_m is porportional to $\sqrt{W/L}$. This is in constrast with the bipolar transistor transconductance (2.19), which is porportional to the polarization current and it is independent from the physical size and geometry of the device.

To compare both g_m typical values of BJT and MOSFET, a MOSFET that operates at $I_D = 1\ mA$, has $k'_n = 20\ \mu A/V^2$, and $W/L = 1$ is considered. The Eq. 2.25 results in $g_m = 0.2\ mA/V$, while a device with $W/L = 100$ has $g_m = 2\ mA/V$. In constrast, a BJT that operates at a collector current of 1 mA has a $g_m = 40$ mA/V. This means, it is very likely that FET technology has limitations to be able to exceed the gain that is achieved using bipolar transistors

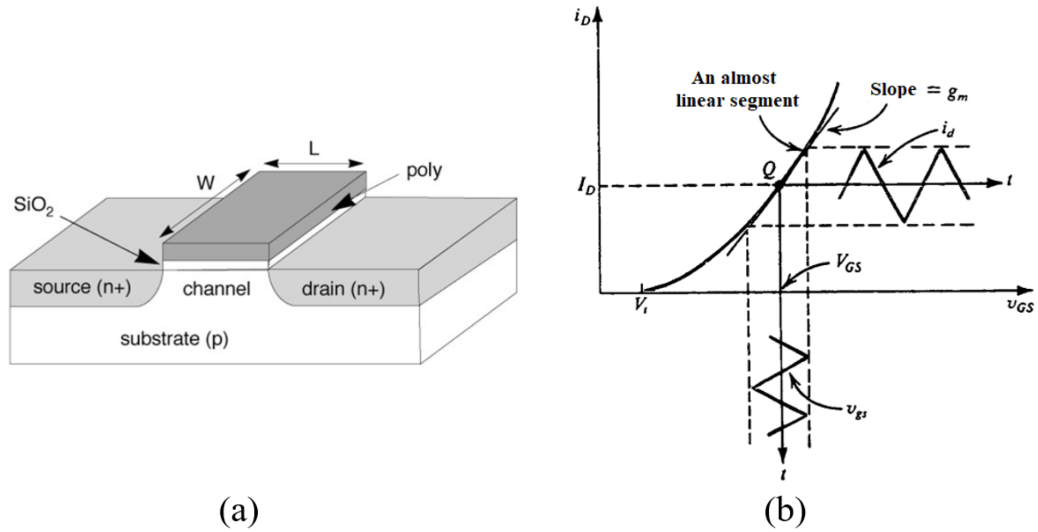


FIGURE 2.11: Operacion del MOSFET bajo condiciones de pequea sea, [18].

Another expression useful for the MOSFET g_m can be obtained by replacing $k'_n(W/L)$ with $2I_D/(V_{GS}-V_t)^2$ (de la Eq. 2.21)in Eq. 2.25:

$$g_m = \frac{2I_D}{V_{GS}-V_t} = \frac{I_D}{(V_{GS}-V_t)/2} \tag{2.28}$$

Therefore, g_m is the ratio between the DC polaritzation current and half the effective voltage ($V_{eff} = V_{GS}-V_t$). Although this expression is similar to the g_m for BJT (Eq. 2.19), there is an important difference. For instance, if we take a typical value from $(V_{GS}-V_t)/2$ fot bipolar transistors, and practical values from $(V_{GS}-V_t)/2$, they are at least 0.1 V or similar. Where, once again, it can be seen that the g_m for BJT is much higher than the one for MOSFET, [18]. However, FET technology offers other advantages, such as ultra-low noise amplification.

2.2.2 Unity current gain frequency and maximum oscillation frequency

The unitary current gain frequency f_t, also known as cutoff frequency, is the frequency where the current gain becomes unity, i.e., $|y_{21}/y_{11}| = 1$. f_t is often used to measure the speed of the device, [37, 39]. The maximum oscillation frequency f_{max} is the frequency where the power gain becomes unity. An example of the

expressions for both these figures of merits is presented in [39] for a microwave CMOS transistor. Based on the small-signal model of the transistor (Fig. 2.12), f_t is defined as:

$$f_t \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.29}$$

To calculate of f_{max}, it is necessary to define the maximum power gain of a device G_{max}. G_{max} is defined as the power gain delivered by a device when both input and output ports are matched to the impedance of the source and load, respectively. This figure of merit provides a fundamental limit on how much power gain it is possible to achieve from a device. For any two-port network, G_{max} is described by:

$$G_{max} = \frac{1}{4} \times \frac{|y_{21}/y_{12}|^2}{Re(y_{11})Re(y_{22}) - Re(y_{21})Re(y_2)} \tag{2.30}$$

By setting $G_{max} = 1$ for this CMOS transistor the expression of f_{max} is:

$$f_{max} \cong \sqrt{\frac{f_t}{8\pi R_{g,i} C_{gd}}} \tag{2.31}$$

An important conclusion is presented in [39], which is that f_{max} varies as $1/W$,

$$f_{max} \propto \sqrt{\frac{1}{W^2 L}}, \tag{2.32}$$

therefore, in order to design for a high f_{max}, shorter devices widths (i.e., W) are desirable. In terms of biasing parameters, Eq. 2.31 predicts that f_{max} is proportional to $\sqrt{g_m}$.

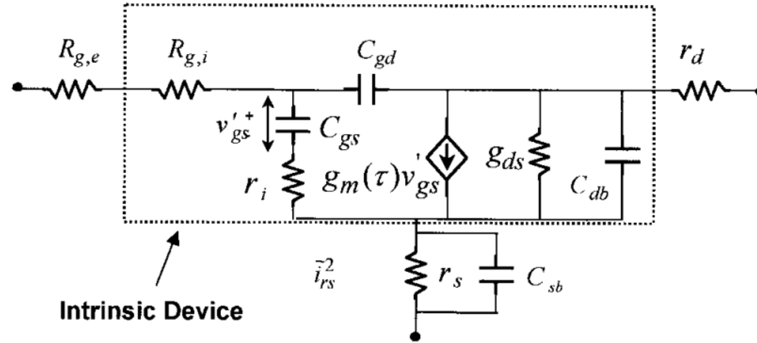


FIGURE 2.12: Small-signal microwave network model of a MOSFET. C_{gd}: gate-drain capacitance, C_{gs}: gate-source capacitance, g_{ds}: output conductance, g_m: output transconductance, r_i: channel charging resistance, τ: transconductance delay, $R_{g,i}$ and $R_{g,i}$ are the gate resistance, [39].

Fig. 2.13 shows f_t and f_{max} as a function of the transconductance for two device widths: 40 and 60 μm. Both f_t and f_{max} are consistent with Eqs. 2.29 and 2.31, respectively. That means that f_{max} is proportional to $\sqrt{g_m}$, and f_t is proportional to g_m. Regarding the device widths, the 40-μm device has relatively higher f_{max} in comparison with the 60-μm device. This is to be expected since the 40-μm device has a smaller gate resistance in comparison to the 60-μm device. Although the f_t curve for the larger device shifts to the right, the relative values of f_t are independent of width. This result is consistent with Eq. 2.29, i.e. since g_m is proportional to W, and C_g ($C_g = C_{gs}+C_{gd}$) is proportional to W, f_t is independent of W, [39].

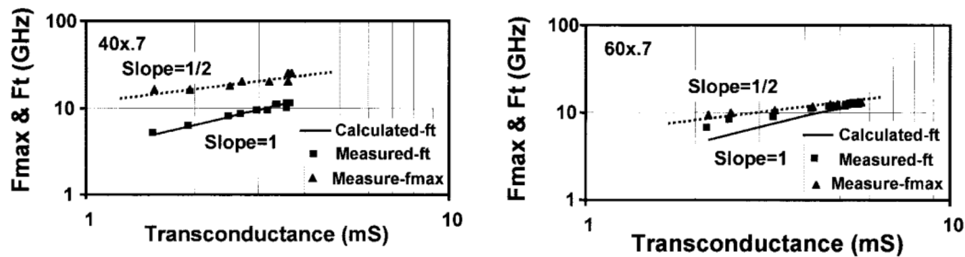


FIGURE 2.13: Experimental and simulated data for the f_t and f_{max} of MOSFET as a function of g_m, [39].

2.3 Passives components and device interconnects

2.3.1 Dielectric constant effect in microstrip line

Microstrip is one of the most common transmission lines for millimeter wave frequencies. Fig. 2.14a shows the geometry of the microstrip line and is composed by a conductor of width W on a thin and grounded dielectric substrate of thickness d with relative permittivity $epsilon_r$. The field lines for this transmission line are shown in Fig. 2.14b.

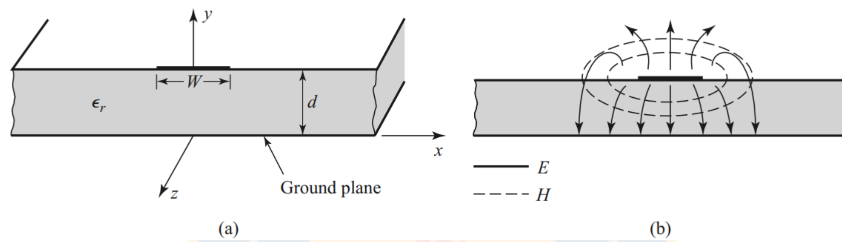


FIGURE 2.14: Microstrip transmission line. (a) Geometry. (b) Electric and magnetic field lines. From [10].

As can be seen in Fig. 2.14b the field lines are not in a region of homogeneous material, where one fraction is in the dielectric region and the other fraction is in air region. This fact makes that the microstrip line unable to support a pure TEM wave since the phase velocity[3] of TEM fields in the dielectric region is $c/\sqrt{\epsilon_r}$, and for the air region is c. Thus, it would be impossible to enforce a phase-matching condition at the dielectric-air interface. The exact fields involved in microstrip line is a hybrid TM-TE wave and for practical applications the dielectric substrate is electrically very thin ($d \ll \lambda$, as in the static DC case), so the fields are quasi-TEM. Consequently, good approximation for the phase velocity (v_p) and propagation constant can be expressed as follows:

$$v_p = \frac{c}{\sqrt{\epsilon_e}} \tag{2.33}$$

$$\beta = k_0\sqrt{\epsilon_e} \tag{2.34}$$

[3]Phase velocity: speed at which a fixed phase point travels on the wave. In free space, the phase velocity equals the speed of light.

Where k_0 is the wave number[4] in free space and ϵ_e is the effective dielectric constant of the microstrip line. ϵ_e takes into account that the field lines are in the dielectric region and some are in the air. This constant can be interpreted as the dielectric constant of a homogeneous medium that equivalently replaces the air and dielectric regions of the microstrip line. ϵ_e can be expressed approximately by:

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/W}} \tag{2.35}$$

Since the microstrip line is not a pure TEM line, the propagation constant is not a linear function of frequency. This means that the effective dialectric constant varies with frequency. Normally, the frequency variation of the effective dialectric constant is more significant than the variation of characteristic impedance (Z_0), both in terms of relative change and the relative effect on performance. The variation in the effective dialectric constant can have a considerable effect on the phase delay through a long section of line, while a small change in characteristic impedance has the primery effect of introducing a small impedance mismatch, [10]. Moreover, a change in line parameters with frequency means that different frequency components of a broadband signal will propagate differently. For example, a variation in phase velocity will make the different frequency components arrive at the output of the transmission line at different times, leading to signal dispersion, and distortion of the input signal. To take into account these effects, approximate formulas have been development. However, numerical computer models are usually more accurate and useful. To show the frequency dependence of the effective dielectric constant the most popular model is presented bellow, [11]:

$$\epsilon_e(f) = \epsilon_r - \frac{\epsilon_r - \epsilon_e(0)}{1 + G(f)} \tag{2.36}$$

Where $\epsilon_e(f)$ represents the frequency-dependent effective dielectric constant, ϵ_r is the relative permittivity of the substrate, and $\epsilon_e(0)$ is the effective dielectric constant of the line at DC (from Ec. 2.35). $G(f)$ is equal to $g(f/f_p)^2$, with $g = 0.6 + 0.009Z_0$ and $f_p = Z_0/8\pi d$ (Z_0 in ohms, f in GHz and d in cm). As can be seen from Ec. 2.39, it start from $\epsilon_e(0)$ with $f = 0$ and then increases toward ϵ_r

[4]Wave number (k): rate at which the wave varies in space and it depends directly on the square root of the dialectic constant of the material. If the wave number increases the wave will move slowly through the material.

as frequency increases. Using this formula, a comparison of the effective dielectric constant is made for alumina ($\epsilon_r = 9.6$) and quartz ($\epsilon_r = 3.8$) substrates. The results are shown in Fig. 2.15. These type of formulas have been developed years before tools for radio-frequency and microwave engineering become available. Such tools usually give accurate results for a wide range of transmission line parameters and today are preferred over closed-form approximations, [10]. In this thesis the Ansys HFSS[5] is used for simulations of 3D millimeter proposed models (in Chapter 5 and 6).

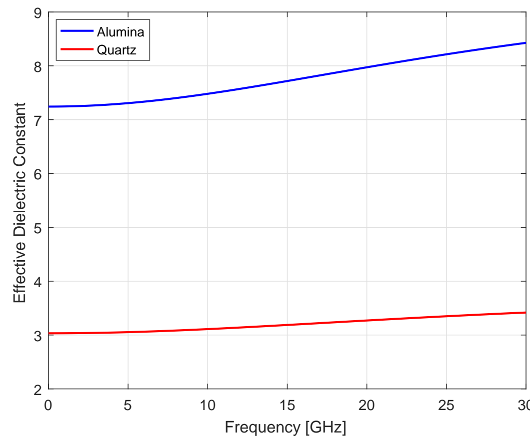


FIGURE 2.15: Effective dielectric constant (from Eq. 2.39) versus frequency for two 50 Ω microstrip lines using alumina ($\epsilon_r = 9.6$) and quartz ($\epsilon_r = 3.8$) substrates.

Attenuation constant (α) is one of the most important characteristic of any transmission line. There are two sources of dissipative losses in a microstrip circuit: substrate loss and conductor loss. The attenuation due to dielectric loss can be calculated as [11]:

$$\alpha_d = \frac{k_0 \epsilon_r (\epsilon_e - 1) \tan \delta}{2\sqrt{\epsilon_e}(\epsilon_r - 1)} \text{ Np/m}, \tag{2.37}$$

[5] Ansys HFSS is a 3D electromagnetic (EM) simulation software for designing and simulating high-frequency electronic products such as antennas, antenna arrays, RF or microwave components, high-speed interconnects, filters, connectors, IC packages and printed circuit boards.

where $\tan\delta$ is the loss tangent[6] of the dielectric. And the attenuation due to conductor loss is approximately calculated as, [11]:

$$\alpha_c = \frac{R_s}{Z_0 W} \text{ Np/m}, \tag{2.38}$$

where $R_s = \sqrt{\omega\mu_0/2\sigma}$ is the surface resistivity of the conductor, ω is the radian frequency, μ_0 is the magnetic permeability of the vacuum and σ is the conductivity of the conductor. Conductor losses are normally larger compared with dielectric losses. However, there may be exceptions with some semiconductor substrates, [10].

The total attenuation losses of the same two 50 Ω microstrip lines used in Fig. 2.15 were calculated using gold and copper as conductors. The total attenuation losses are shown in Fig. 2.16. From these results it is possible to observe that the attenuation is increasing with the frequency. Furthermore, if the dielectric constant is increased the attenuation will also increase. In this regard, it should be mentioned that the conductor to be used is sometimes imposed by the manufacturing company's process. Therefore, the only material that we could modify to get a better performance is the dielectric material.

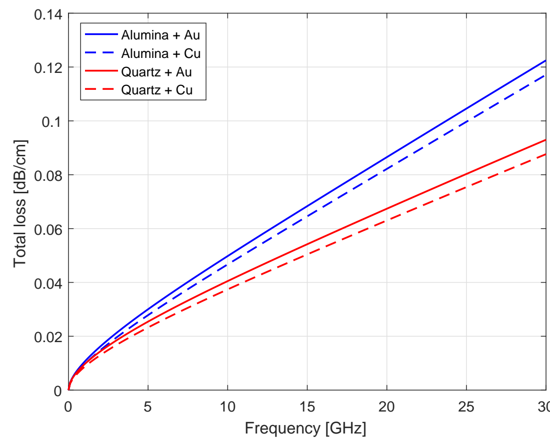


FIGURE 2.16: Total losses ($\alpha_d + \alpha_c$ from Eqs. 2.37 and 2.38, resp.) for the two 50 Ω microstrip lines used in Fig. 2.15. For both transmission lines gold and copper conductors were used.

[6]Loss tangent is the measure of signal loss due to the inherent dissipation of electromagnetic energy in the substrate. It is seen to be the ratio of the real to the imaginary part of the total displacement current. Microwave materials are characterized by specifying the real dielectric constant ϵ_r and the loss tangent at a certain frequency, [10].

2.3.2 Waveguide-to-microstrip probe transitions

When a monolithic microwave integrated circuit, MMIC[7], is manufactured (Fig. 2.17a), its performance must be measured on-wafer (Fig. 2.17b) to verify that it works as was predicted by the previous simulations. If the chip works well, it must be installed in a metallic support so that it can be connected in a real environment, one in which the chip was designed for, a radio-astronomy receiver, for example. One of these metallic supports, or more commonly called package or block, is shown in Fig. 2.17d. In Fig. 2.17e, a real environment where the chip will be used is shown. In this figure, the device under test (DUT) are the packaged MMIC. The design to get a completely assembled chip involves all the components needed to provide the RF input signal, an output for the RF output signal of the chip and the all the DC signals needed to energize the active devices inside the chip. A MMIC mounted inside of the package is shown in Fig. 2.17c. It should be mentioned that in this figure the top cover is removed.

As can be seen in Fig. 2.17c, the input and output of the package are rectangular waveguides. Microwave technology is looking for the miniaturization and integration, for this reason modern circuitries are manufactured using planar transmission lines, such as microstrip and coplanar rather than waveguides. However, there are many applications where waveguides are needed. This thesis is one of those cases, where the signal, for example, can come from a horn with its output in a rectangular waveguide form (Fig. 2.18). The hollow rectangular waveguide can propagate TM and TE modes, but not TEM waves since only one conductor is present. The TE_{01} is the dominant mode, which means, it has the lowest cutoff frequency and it is dominant even over the TM modes, [10]. Due to the practical importance of the TE10 mode, in the vast majority of waveguide applications, the operating frequency and guide dimensions are chosen so that only the dominant TE_{01} mode propagates. Fig. 2.19 shows the geometry of a rectangular waveguide and the expression for the cutoff frequency of TE_{01} mode is, [10]:

[7]Monolithic literally means "one rock" and, in electronics, has come to refer to the processing of active and passive components in situ on a semiconductor slab, providing interconnections to the components to form an integrated circuit (IC), [22]. A monolithic microwave integrated circuit (MMIC) is an active or passive microwave circuit formed in situ on a semiconductor substrate by a combination of deposition techniques including diffusion, evaporation, epitaxy, implantation and other means, [23]. These should not be confused with the microwave integrated circuits (MICs), which are a hybrid device with one layer of metallization for conductors and transmission lines, with discrete components (resistors, capacitors, integrated circuit chips, transistors, diodes, etc.) placed and bonded to a substrate which can be a high performance PCB or Alumina.

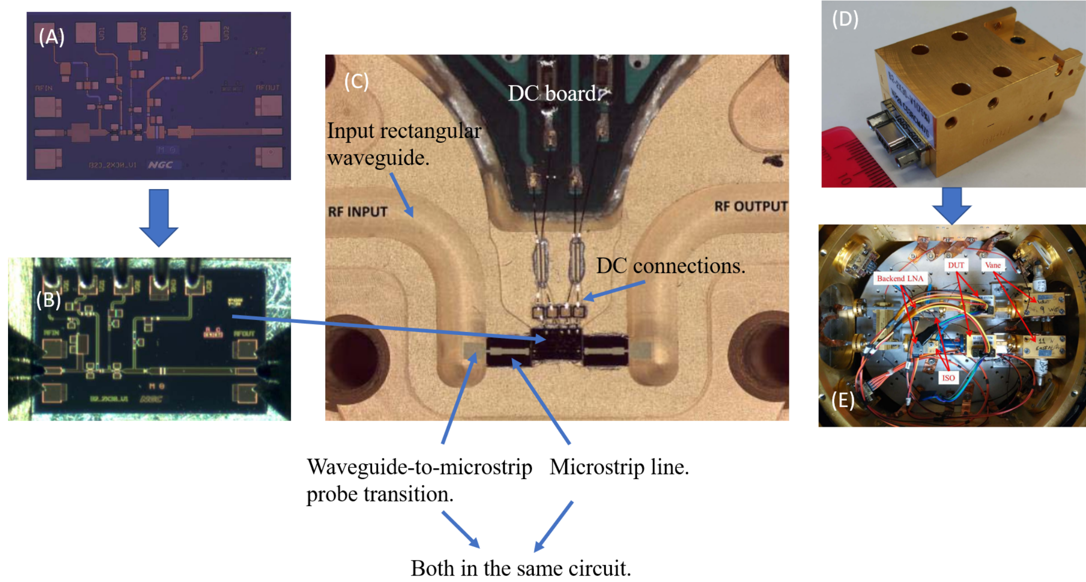


FIGURE 2.17: From [55]: (a) Microscopic photograph of a fabricated MMIC, (b) cryogenic probing of a MMIC, (c) interior of a WR-10 LNA block, (d) exterior of a WR-10 LNA block and (e) interior of the Dewar with setup for characterizing two LNA blocks.

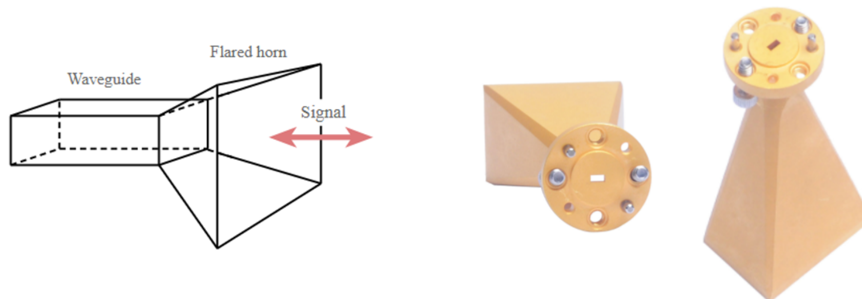


FIGURE 2.18: Left: horn diagram, [20]. Right: two different views of a real horn.

$$f_{c_{01}} = \frac{1}{2a\sqrt{\mu\epsilon}} \tag{2.39}$$

It is a standard convention to have the longest side of the waveguide along the x-axis, such that $a > b$. The Electronic Industries Alliance (EIA) developed standards for the rectangular waveguide dimensions to ensure the equipment of different manufacturers was compatible and interchangeable. Some of these standards are, for example, the dimensions for the frequency band from 75 to 110 GHz, shown in Table 2.1.

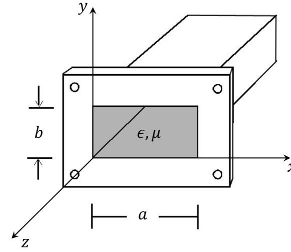


FIGURE 2.19: Geometry of a rectangular waveguide.

Recommended Frequency Band:	75 to 110 GHz
Cutoff Frequency of Lowest Order Mode:	59.015 GHz
Cutoff Frequency of Upper Mode:	118.03 GHz
Dimensions:	A = 0.1 Inches [2.54 mm], B = 0.05 Inches [1.27 mm]

TABLE 2.1: Standart dimensions for the frequency band of 75-110 GHz, named WR-10, [76].

To perform the transition from rectangular waveguide to microstrip line, the common E-plane probe designs ([30], already seen in Fig. 2.17c), were used in this thesis. For this type of probe, the substrate surface aligns along the direction of propagation of the waveguide (Fig. 2.20). This configuration has been successfully used to mount MMIC chips up to at least 300 GHz, [30]. The place where this probe is mounted has an open window in the broadwall of the rectangular waveguide (Fig. 2.20 may clarify this). The E-plane probe design are well described in [21]. This work establishes, based on Fig. 2.20, that the width and height of the window opening at the broadwall were first fixed based on easy assembly requirements, and to ensure that the waveguide modes are in cut-off condition along the direction of propagation towards the microstrip line. For the designing of the probe, a parametric study was carried out to define the parameters of: the probe width, the probe length and the back-short distance, taking into account how these parameters will affect the impedance ($Z_0 = R + jX$) vs frequency of the probe, as seen in the plane of the broadwall window. This study was performed using different dielectric constants (ϵ_r from 2.1 to 13). For ϵ_r greater than 2.2, the impedance has a real part of less than 50 Ω and a capacitive series reactance. A high impedance inductive line is used first in series to resonate out the capacitive reactance. This is followed by a quarter-wave impedance transformer to match the real part of the probe impedance to 50 Ω. Based on Fig. 2.20 five design were proposed for a WR-10 waveguide block, see Table 2.2. These probe designs can be applied to any waveguide size with a width/height aspect ratio of 2:1 by

multiplying the dimensions listed in Table 2.2 by a scale factor equal to (width of the target waveguide in um)/2540.

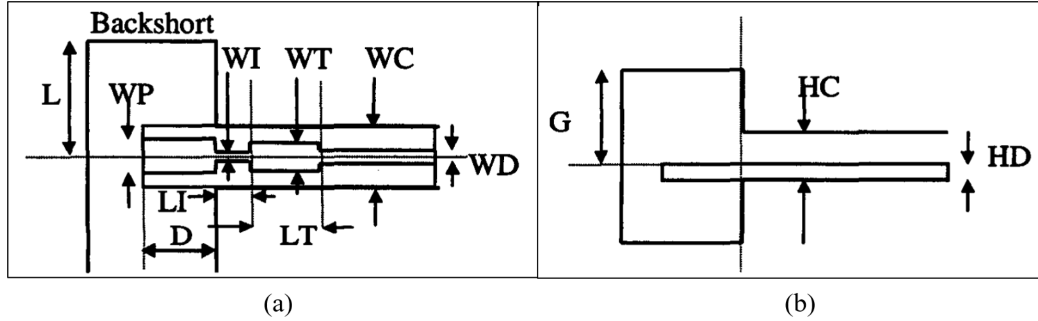


FIGURE 2.20: From [21]: Common E-plane probe transition in the longitudinal configuration. (a) View of waveguide narrow wall (b) View in direction of propagation towards backshort.

#	Probe	ϵ_r	L	HC	HD	WC	WP	D	WI	LI	WT	LT	G	WD
1	Teflon-127	2.2	838	259	127	973	324	635	80	100	-	-	1270	230
2	Teflon-76	2.1	838	254	76	508	230	660	120	260	-	-	1270	210
3	Diel6-127	6.0	876	259	127	740	291	600	80	100	180	420	1270	140
4	Alumina-100	10.1	876	259	100	508	200	600	50	100	130	350	1270	80
5	GaAs-100	13.0	908	259	100	740	259	560	40	60	130	320	1270	70

TABLE 2.2: Reproduced from [21]: Longitudinal probe (Fig. 2.20) dimensions for substrates of 4 different dielectric constants. All units are in um and are for WR-10 waveguide.

2.3.3 Interconnections between microwave circuits and coefficient of thermal expansion

This section presents three types of techniques that are possible to use when a connection is required between microwave circuits. The first isthe wire-bond which is the most commonly used over time. Then the flip-chip technique will be reviewed, as this technique has increased its use at millimeter-wave frequency. A more sophisticated technique, called membrane, will be explained along with the reason why it is very promising for higher frequency receivers. Finally, the coefficient of thermal expansion of the material is reviewed.

2.3.3.1 Wire-Bonds

Wirebonding is one of the most important invention of the electronics industry and is the heart of first level die-to-substrate interconnects technology in semiconductor packaging, [25]. This technique is employed to connect solid-state devices with passive circuits, as well as multichip modules. A diagram and a millimeter wave implementation example of this technique is shown in Fig. 2.21. Fig. 2.22 shows an example of the wire bonding process and a wire bonding machine. The wire-bond technique has demonstrated good performance at low frequencies. However, for higher frequencies the technique introduces large parasitic inductive reactances, which will decrease the performance of the system. For example, the behaviour at millimeter wave frequencies is determined by the fact that, as frequency is increased, the lenght of the wires reaches significant transmission line properties. In the case of coplanar bond wires to connect the center conductors as well as the ground planes, a suitable model proposed in [26] that takes into account this behaviour is the raised coplanar waveguide, see Fig. 2.23a. In this model, the shapes of the ground and center conductor are given by the cross-section of the bond wires, and the substrate is composed of an air layer of thickness h, which is either grounded by a metallic surface or located on top of a dielectric layer, corresponding to a mounting substrate. The insertion loss (simulated and measurements) and return loss (simulated) using this model are shown in Fig 2.23b. The decreased performance is increased by the number of the wires used in the interconnection, and also by the length of the wires, [26–28, 31]. The length of the wires depends in part on the proximity between the circuits (d_{chips} in Fig. 2.21a) to be interconnected, which adds an uncontrolled variable to its implementation.

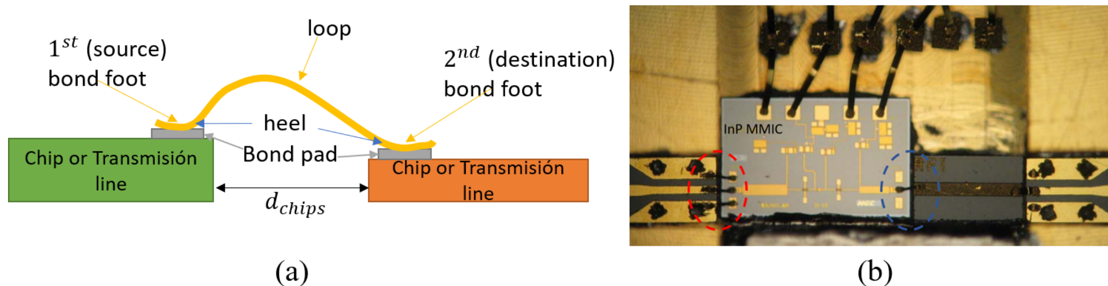
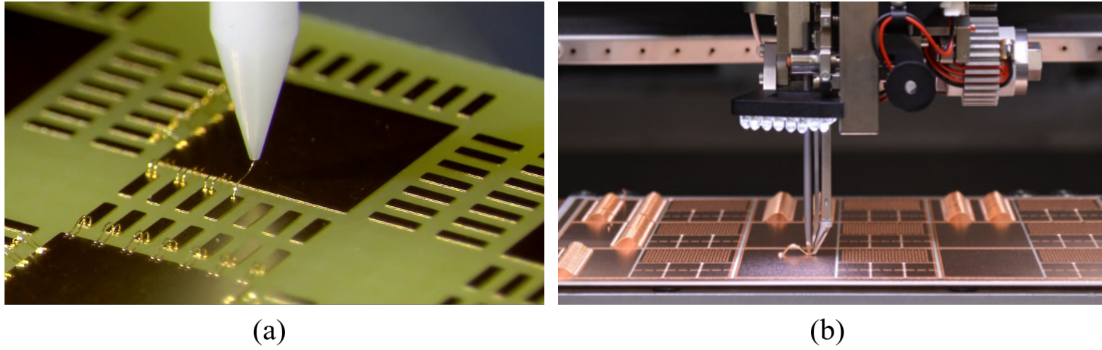


FIGURE 2.21: (a) Wire-bond connection diagram. (b) InP MMIC connected to two circuits using wire bonds. On the left (red circle), it is linked in coplanar mode, and on the right (blue circle), it is linked in microstrip mode, [44].



(a) (b)

FIGURE 2.22: (a) Manufacturing of wire bond. (b) Wire bonding machine.

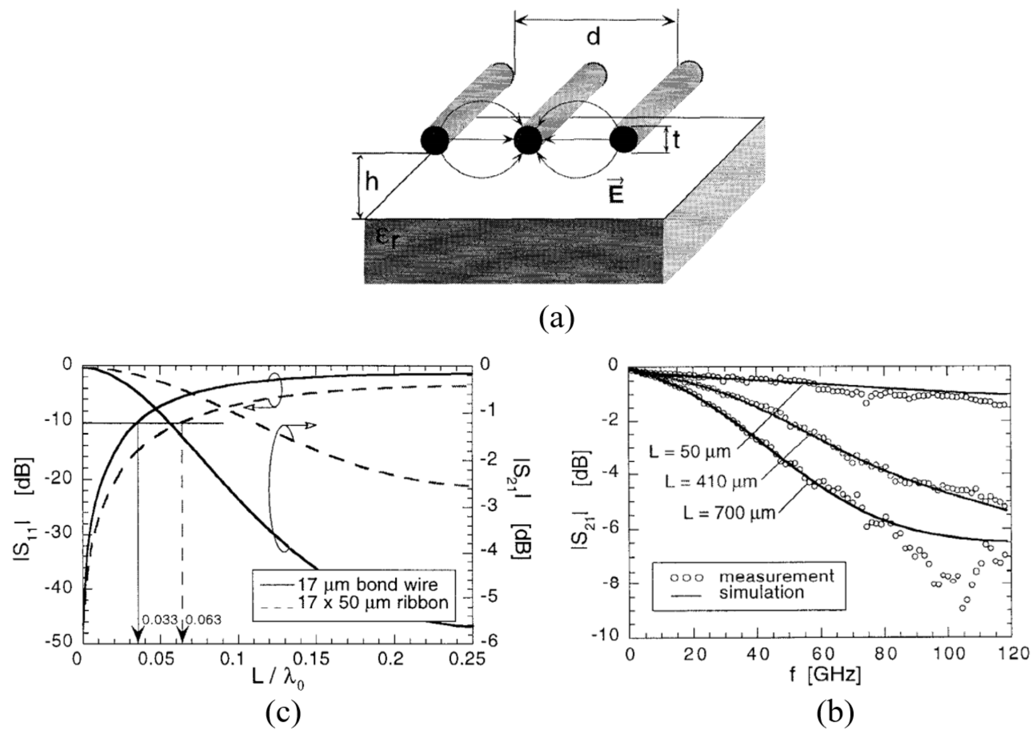


FIGURE 2.23: From [26]. (a) Raised coplanar waveguide model. (b) Measured and stimulated insertion loss vs frequency for bond wire interconnections of different lengths. (c) Simulated return loss and insertion loss of bond wire and bond ribbon interconnection vs normalized wire length L/λ_0.

2.3.3.2 Flip-chip

Flip-chip transitions has become the direct alternative to overcome the challenges introduced by wire bonds interconnects at higher frequencies. Flip-chip makes the system much more flexible since the locations of the input and output lines of the signal are no longer restricted to the perimeter of the chip, as they are when

using the wire bonds. Flip-chip has two key advantages: 1) it is small in terms of dimensions as well as electrical size, and 2) its relevant parameters (height and diameter) can be well controlled, [31]. A diagram of the flip-chip interconnect is shown in Fig. 2.24 together with an image of cross-sectional view of an Au bump, and a image of a manufactured Flip-chip interconnect structure. Common bump diameters are in the 20–80-μm range. They can be made with good control of height and average diameter, which results in an electrically small interconnect and a module with reproducible performance, [31]. The small dimensions of the flip-chip interconnect make it differ significantly from that of the classical mounting technique using wire bonding, where the bonding wire causes a relatively large parasitic inductance. Fig. 2.25a shows the calculated return loss and insertion loss for the single flip-chip transition of Fig. 2.24a as a function of the bump height (h_b). The comparison with the performance of bond wire interconnections in Fig. 2.23c immediately reveals the electrical superiority of the flip-chip technology. Insertions loss below 0.5 dB are achieved even at frequencies beyond 100 Ghz, while the return loss indicates that no additional matching is needed, [26]. In the line of the impedance matching, one thing to keep in mind when designing the pads, on the motherboard (where the chip is flip-chipped) and on the chip, is that they cause dielectric loading of the transition, which can be identified as the main source of the reflections (see Fig. 2.25b), [31]. Therefore, as a first step, the pads should be kept as small as possible to achieve maximum return loss at the interconnect.

An effect to take into account when designing an flip-chipped system is the chip detuning. This effect can significantly influence the electrical properties of the chip and is produced by the proximity between the active surface of the chip and the motherboard, where only an air gap as thick as the bump height separate both component. The actual amount of detuning depends on the element type, the size and the spacing between chip and motherboard, which is controlled by the bump height. Large bump heights minimize detuning. Particularly sensitive to detuning effects are transmission lines and spiral conductors, while transistors and small-sized components do not show a noticeable influence, [31]. Using a underfiller ([32]), the detuning effect is more pronounced since the dielectric material is in direct contact with the chip. This problem can be addressed by including detuning in the chip design a priori, or by having a relatively thick dielectric layer on top of the chip so that the influence of underfilling is more or less negligible.

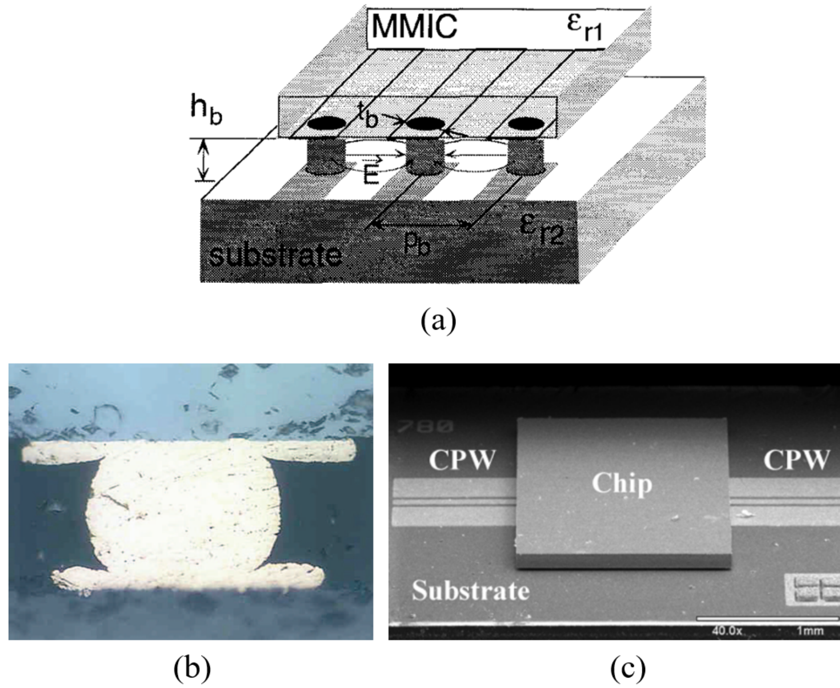


FIGURE 2.24: (a) Diagram of flip-chip interconnection of coplanar MMIC, [26]. (b) Cross-sectional view of an Au bump, [31]. (c) manufactured flip-chip interconnect structure, [32].

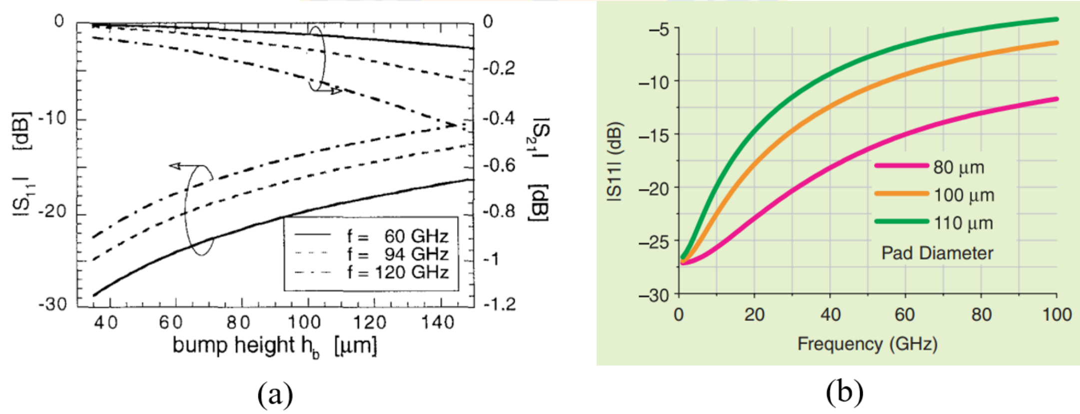
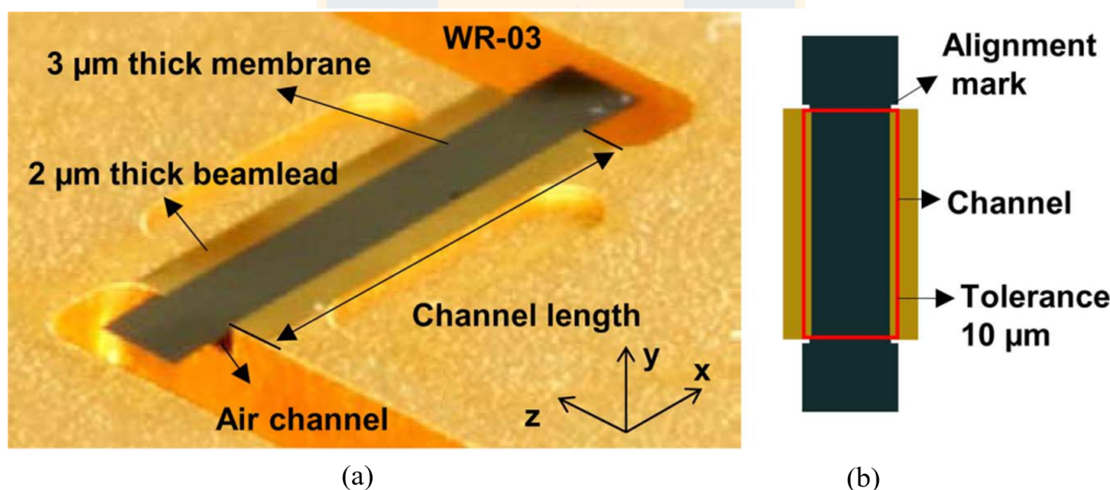


FIGURE 2.25: (a) Simulated return loss and insertion loss of a single flip chip transition using the bump diameter $t_b = 40\mu m$ and the bump pitch $p_b = 90\mu m$ as a function of the bump height h_b, [26]. (b) Simulated influence of pad size ($80\mu m$ bump height, $100\mu m$ pad size): reflections at the flip-chip interconnect against frequency with pad size as parameter, [31].

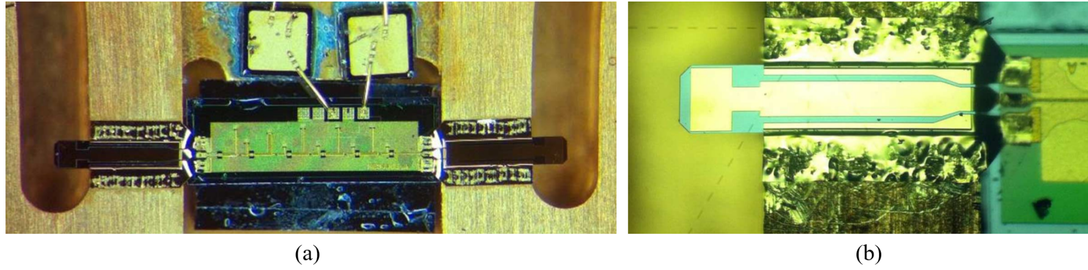
2.3.3.3 Membrane

The membrane transition is a novel technique recently used for first time in transistor-based IC technology circuits, [34]. Membrane technology have demostrated excellent transmission characteristics and return loss for frequencies as high as the 220-325 GHz band, [34, 35]. One of the first implementation is shown in Fig. 2.26. This implementation is an E-plane split block where a membrane circuit is mounted. As can be seen, in this technique the circuit is aligned in a predefined channel and is suspended in an air channel formed by two symmetrical block halves. The beam leads that are clamped in the blocks provide mechanical support, as well as a well-defined ground connection, which offers a RF return current path with low inductance, [35]. When this technique is used to design E-plane probe transitions as in [34] (see Fig. 2.27), the beam leads are “glued” to the to the circuit pads by pressuring them with a wedge in a standard bonding machine.



(a) (b)

FIGURE 2.26: From [35]. (a) Photo of a membrane circuit mounted on air-channel in a half E-plane split block. (b) Shape of the membrane, the red rectangular shows the position of the air-channel.



(a) (b)

FIGURE 2.27: From [34]. (a) Microphotograph of a InP MMIC in block housing with membrane transitions. (b) Microphotograph of the waveguide transition on GaAs membrane substrate with the ground-signal-ground connection.

2.3.3.4 Coefficient of thermal expansion

The main challenges for packaging low-temperature electronic components are the changes in material properties as a function of temperature and stresses induced by differences in the coefficients of thermal expansion (CTE) of materials, [36]. If the CTEs of the materials do not match, the structure will warp when it cools down. The stresses within the materials are proportional to: the differences in CTE, the modulus of elasticity of the materials, the dimensions of the materials and the ΔT between the joint and the operating temperatures. Low operating temperatures correspond to large ΔT and higher stresses for a given assembly compared to commercial operating temperatures. Repetitive thermal cycling (and deformation) will lead to fatigue failure of the die joint welds. Large ΔT thermal cycling is one of the main challenges for low temperature electronic packaging. Finally, assembly processes and manufacturing defects also influence survival.

Material	Si	AlN	Al_2O3
CTE [ppm/°C]	2.9	4.5	7.2

TABLE 2.3: Coefficient of thermal expansion for silicon (Si), aluminum nitride (AlN) and alumina (Al_2O3). [36].

Therefore, in the case of this thesis work, this factor will have to be taken into consideration when designing the transitions between the probes and the silicon circuits. Table 2.3 shows the CTE for three different materials. In case a substrate is needed for a silicon chip, a material that has a similiar CTE must be found. By

observing Table 2.3, it is possible to verify that AIN would provide a better CTE match to silicon than alumina. Custom AlN substrates are a viable, but costly option. Alumina substrates are widely available and were chosen as the package material, [36].

3 Active devices

In radio astronomy observations, celestial signals must be detected in the presence of noise from the receiver, as well as extra radiation from the ground, the atmosphere, the sidelobes of the antenna, etc. These celestial signals are in general very weak, for example, the ones coming from cosmic microwave background radiation are at 2.726 K, [52], which is translated into very low power levels in a given range of frequency, see Eq. 2.1. A large part of a system noise temperature (T_{sys} from Eq. 2.3) is commonly constituted by the receiver noise temperature (T_{rx}). For this thesis work, the required frequencies are in the range of millimeter wave frequencies. In this range, as was mentioned in Chapter 1, HEMTs have demonstrated the best noise performance and for that reason they are part of the state of the art in radio astronomy receiver at these frequencies, [2, 53]. However, to achieve the desired noise levels, it has been necessary to cool these devices to cryogenic temperatures for two main reasons: device performance improvement, usually due to electron transport improvements, and reduction of the influence of the thermal noise generated by parasitic elements, [3]. After that, a review of the architecture of the most used and promising devices for use in millimeter wave cyogenic systems will be presented. In addition, the state of the art of silicon-based devices for milimeter waves is presented.

3.1 Transistors for millimeter-wave cryogenic applications

3.1.1 High electron mobility transistors

High electron mobility transistors (HEMTs) or also called heterojunction field effect transistors (HFETs) are a type of field effect transistors, FETs. Its importance for millimeter and submillimeter wave receiver systems lies in the low levels of intrinsic noise that it has demonstrated at these frequency levels, [3, 4]. In these transistors the electrons or charge carriers propagate in a channel of a very small size. In this channel the electrons move at very high speeds. The channel is formed at the interface of two semiconductor materials. The use of two materials is what gives it the name of heterostructure in its second name. For example, early HEMTs used GaAs and AlGaAs as the two materials. AlGaAs contributes electrons. These diffuse only a small distance in GaAs due to the positive space charge in AlGaAs. In this way the electrons are confined in a narrow shell (previously referred to as a small channel) which is a potential well (or quantum well [1]). This confinement is called a two-dimensional electron gas, or "2 DEG". Since the carriers are located in the 2 DEG region where there are no doped ions, there is less scattering and therefore high electron mobility and less noise. One of the fastest materials for the manufacture of HEMTs is indium phosphide (InP), using $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Ga_{0.48}As$. The conduction band at the interface of these materials forms the potential well, which is triangular in shape and is where the electrons are confined, in this case in the layer of $In_{0.53}Ga_{0.47}As$, [30].

In Fig. 3.2 the energy band diagram for this HEMT is shown in detail. The potential well from the point of view of energy bands occurs due to the different band gaps and their relative alignment to each other once joined. This junction produces band discontinuities at the interface between the two semiconductors, Fig. 3.2a. These discontinuities are called the valence and conduction band offsets ΔE_c and ΔE_v, see Fig. 3.2b. By choosing the right materials and their compositions, the displacement of the conduction band can form a potential well of triangular

[1] A quantum well is the name given to a potential well (which is the region that surrounds a local minimum of potential energy) that confines, in two dimensions, particles that were originally free to move in three, forcing them to occupy a limited area. This effect happens through the use of a confining potential due to band gap differences with a surrounding matrix material or with electric field gradients, [29].

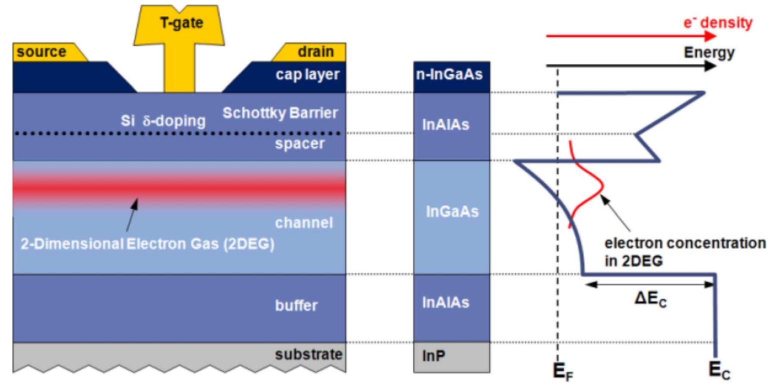


FIGURE 3.1: Typical InP HEMT side view, layer structure, and side view energy band diagram, reproduced from [30].

shape that limits electrons in the horizontal direction. Inside the well, electrons can only move in a two-dimensional plane parallel to the heterointerface, which is given the name seen before 2 DEG region.

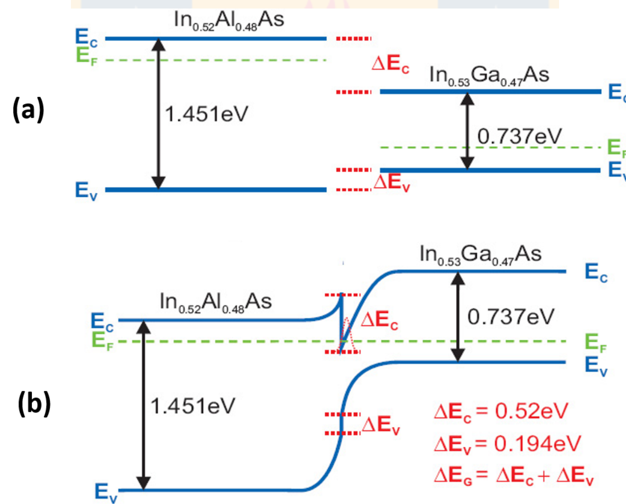


FIGURE 3.2: (a) Diagram of the band structures of InAlAs and InGaAs at equilibrium. (b) Semiconductors in contact at the equilibrium. A 2DEG is formed at the interface in the triangular shaped well, [45].

To increase g_m, the channel material can be made more mobile (higher indium content) and the gate length reduced. The speed of a HEMT transistor can be measured by measuring the transistor parameters with a network analyzer and calculating the cutoff frequencies of the transistor, the cutoff frequency of the current gain and the maximum frequency of oscillation. Both figures of merit are used to predict the highest operating speed of the transistor.

3.1.1.1 Model for cryogenic temperature

Noise properties of FETs (HEMTs) have been studied considering the fundamental equation of transport in semiconductors, but none of these models have been used to explain the performance of FETs at cryogenics temperatures, [3]. Meanwhile, a model that describes very well the noise properties of FETs versus frequency, temperature and transistor bias was proposed by Pospiesalski, [42]. Although this modeling does not provide any insight into the nature of the noise generation mechanism in the device, it offers a way for designers to achieve the best noise levels of a FET, relating the minimum noise temperature to the elements of an equivalent circuit of a FET, Fig. 3.3. In this modeling, parasitic resistances contribute only thermal noise and, with knowledge of the ambient temperature T_a, their influence can be easily taken into account. The noise properties of an intrinsic chip are then treated by assigning equivalent temperatures, T_g and T_d, to the remaining resistive (frequency-independent) elements of the equivalent circuit, r_{gs} and g_{ds} respectively. No correlation is assumed between noise sources represented by the equivalent temperatures T_g and T_d. Therefore, in addition to elements of an equivalent circuit, the temperatures T_g, T_d and T_a need to be predicted for the noise parameters at any frequency, temperature, and bias in the frequency range, in which $1/f$ noise and noise caused by the gate leakage current are negligible, [3]. These noise parameters are four and their approximate expressions of an intrinsic chip are:

$$R_{opt} \cong \frac{f_t}{f}\sqrt{\frac{r_{gs}T_g}{g_{ds}T_d}} \tag{3.1}$$

$$X_{opt} = \frac{1}{\omega C_{gs}} \tag{3.2}$$

$$g_n = \left(\frac{f_t}{f}\right)^2 \frac{g_{ds}T_d}{T_o} \tag{3.3}$$

$$T_{min} \cong 2\frac{f}{f_t}\sqrt{g_{ds}T_d r_{gs}T_g} \tag{3.4}$$

or

$$T_{min} \approx \frac{f}{f_{max}}\sqrt{T_g T_d}, \tag{3.5}$$

which are valid if

$$\frac{f}{f_t} \ll \sqrt{\frac{T_g}{T_d}\frac{1}{r_{gs}g_{ds}}}, \tag{3.6}$$

where

$$f_t = \frac{g_m}{2\pi C_{gs}} \tag{3.7}$$

$$f_{max} = f_t\sqrt{\frac{1}{4g_{ds}r_{gs}}} \tag{3.8}$$

R_{opt} and X_{opt} are the real and imaginary parts of the optimum source impedance, T_{min} is the minimum noise temperature of a chip, g_n is the noise conductance, f_t is the transistor cut-off frequency, and f_{max} is the maximum frequency of oscillations. An example of the good accordance between the predicted noise and gain of the model and their measurements are shown in Fig. 3.4. In these results, it is possible to observe the improvement on the noise performance when the device is cooling to cryogenic temperature.

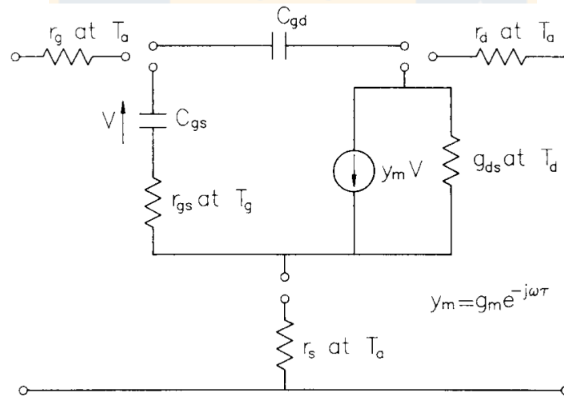
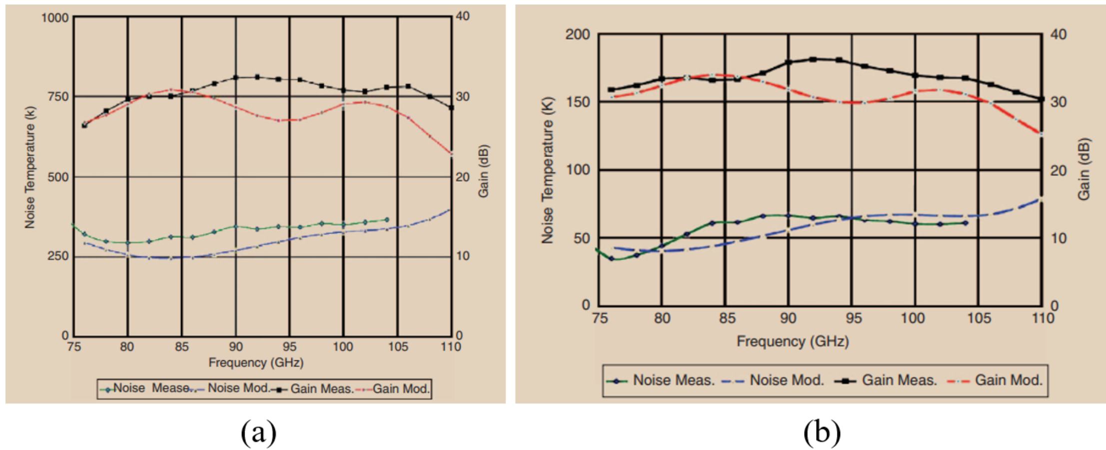


FIGURE 3.3: Equivalent circuit of FET (HEMT) chip, [42].



(a) (b)

FIGURE 3.4: A comparison of measured gain and noise characteristics of a W-band amplifier with model prediction at room temperature (left) and cryogenic temperature (right), [43].

3.1.2 CMOS transistors

Silicon-on-insulator (SOI) CMOS technology has been widely used in the development of millimeter wave low noise amplifiers, [5, 68, 82]. SOI technology is an answer to the problems with conventional Bulk substrates (Fig. 3.5a), which, as device sizes continue to shrink, a large number of problems develop such as high leakage current, high power dissipations, transistor performance degradation and reduced reliability. In SOI technology, transistors are manufactured by placing a thin insulating layer, such as silicon oxide, between a thin layer of silicon and the silicon substrate, Fig. 3.5b. One of the typical mechanisms of SOI CMOS transistors is the Fully Depleted Silicon On Insulator (FD-SOI, see Fig. 3.5b), in which an ultra-thin layer of insulator is placed on the silicon base. Then, a very thin silicon film implements the channel of the transistor. Thanks to its thinness, there is no need to dope the channel, thus making the transistor Fully Depleted. By construction, FD-SOI enables much better transistor electrostatic characteristics versus conventional bulk technology. The buried oxide layer lowers the parasitic capacitance between the source and the drain. It also confines efficiently the electrons flowing from the source to the drain, dramatically reducing performance-degrading leakage currents, [48, 49]. SOI CMOS transistors have reached very high f_t and f_{max} above 400 GHz, [50, 82].

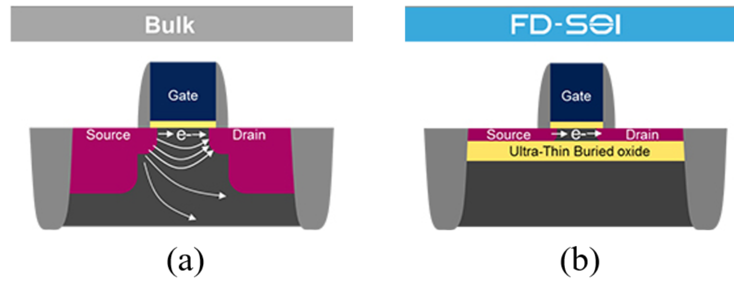


FIGURE 3.5: From [48]: Diagram of CMOS (a) conventional Bulk and (b) FD-SOI technology.

3.1.2.1 Model for cryogenic temperature

The behaviour of CMOS transistor at cryogenic temperatures was very well modeled in [68], see Fig. 3.6a,b. This modeling employs the Pospieszalski noise model, [42], with the assumption that T_d is equal to the ambient temperature, T_a and the T_d depend upon drain current density, but is insensitive to ambient temperature. This study mentions that the bias is typically reduced in cryogenic applications, and that this also corresponds to the current density to achieve near peak f_{max} operation at cryogenic temperatures. It is a significant improvement in f_t and f_{max} when cooling the device from 293 to 6 K. The peak values improve from 268 to 317 GHz, and 289 to 511 GHz, respectively. The study mentions this is so because at a fixed bias, the extracted capacitance and g_{ds} values are only weakly temperature dependent, whereas resistances and transconductances improve significantly with cooling (see Eqs. 3.7 and 3.8). Thus, the improvement in f_t is primarily due to an increase in the ratio of g_m to the capacitances, whereas the improvement in f_{max} is also influenced by a significant drop in the series and r_{gs} resistances. The behaviour of T_{min} when cooling (Fig. 3.6c) the device from 293 to 6 K is dominated by r_{gs} and T_a. The temperature dependence of the extrinsic resistances r_g, r_d and r_s will have a similar effect to r_{gs}. Fig. 3.6c,d shows the improvements of T_{min} regarding the physical temperature and frequency. f_t, T_d and g_{ds} were found to be relatively independent of temperature. R_{opt} decreases significantly with cooling, since both $r_{gs}T_g$ and r_{gs}^2 (see Eq. 3.1 and Eq. 11 from [42]) are observed to decrease significantly with cooling. The good agreement between the measured and modeled small-signal performances presented in [68] are shown in Fig. 3.6a,b.

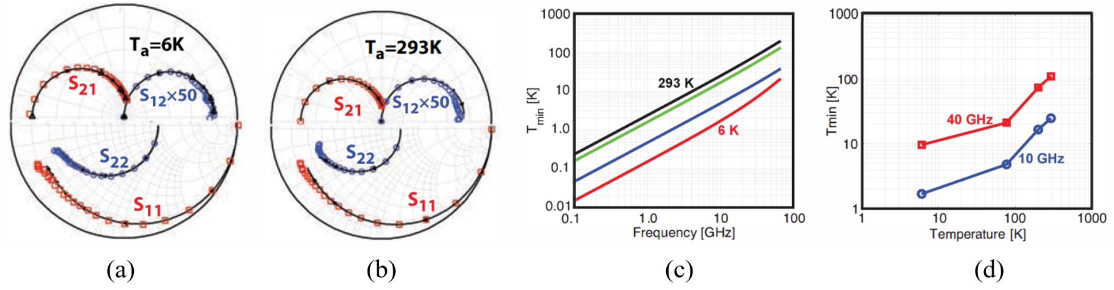


FIGURE 3.6: From [68]: Model verificaion of a CMOS transistor in the frequency range of 0.01–67 GHz: (a) $T_a = 6$ K and (b) $T_a = 293$ K (solid lines repesent model and dashed lines represent measurement). (a) Frequency dependence of T_{min} for physical temperature of 6 K (red),77 K (blue),200 K (green),and 300 K (black). (c) Temperature dependence of T_{min} for 40 GHz (red) and 10 GHz (blue).

3.1.3 Heterojunction bipolar transistors

Heterojunction bipolar transistors (HBTs) are a type of bipolar junction transistor (BJT), but unlike BJT, it uses different semiconductor materials to fabricate the transistor. The purpose of using different materials is to generate a variation in the energy bands that facilitate the mobility of the charge carriers from the emitter to the collector. The energy bands are varied by doping with impurities from materials other than the base substrate to form the heterojunctions. For example, Fig. 3.7 shows the difference between a silicon BJT transistor and a SiGe HBT, which the base graduated using the germanium semiconductor. Fermi levels [2] are indicated by dotted lines in each region of the diagram. This makes its energy diagram facilitate the mobility of the charge carriers towards the collector of the transistor, managing to increase its frequency response.

Another important point of this technology is that it is possible to integrate it with silicon CMOS processes, achieving BiCMOS technology. It is possible to implement this technology in commercial CMOS processes and thereby develop high-frequency technology at low cost. Fig. 3.8 shows a high performance HBT transistor using InP substrate and its band diagram.

HBTs have reached maximum oscillation frequencies beyond 1 THz, Fig. 3.9a. This was using the indium phosphide semiconductor as a substrate, which has

[2]The Fermi energy is defined as the energy of the topmost filled level in the ground state of the N electron system. The ground state is the state of the N electron system at absolute zero, [40].

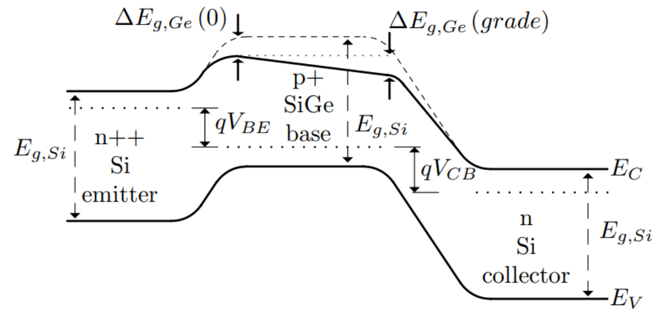


FIGURE 3.7: Band Diagram for a SiGe HBT indicating deviation from that of a pure silicon transistor, [41].

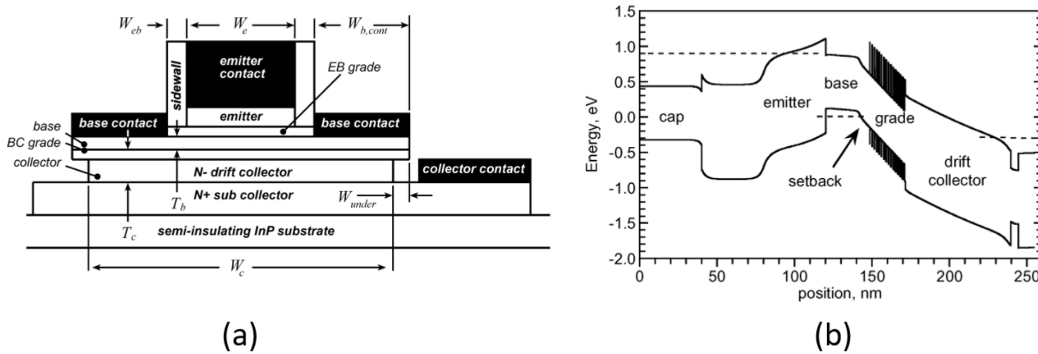


FIGURE 3.8: (a) HBT cross-section. (b) HBT layer structure and band diagram. The emitter cap is InGaAs, the emitter InP, the base and setback layer are InGaAs, the grade an InAlAs/InGaAs superlattice, and the drift collector and subcollector InP.

higher electron mobility than silicon. However, recent developments in HBT using silicon as a substrate are also reaching these frequency levels, Fig. 3.9b.

3.1.3.1 Model for cryogenic temperature

The modeling of SiGe HBT performance for cryogenic temperatures is very well developed in [41, 64]. This model is based on the experimental extraction of the small-signal parameters, Fig. 3.10. There are four additional components included in the intrinsic HBT, they are: a) $r_b = r_{bx} + r_{bi}$, which is required to model the resistance of the polysilicon extrinsic base, as well as that of the SiGe intrinsic base; b) r_e, which is needed to model the polysilicon emitter; c) r_c, which is needed to model the parasitic collector resistances; and d) C_{CS}, which is a depletion capacitance between the collector and the ground that arises due to the fact that the collector was deposited on a semiconducting substrate. The experimental

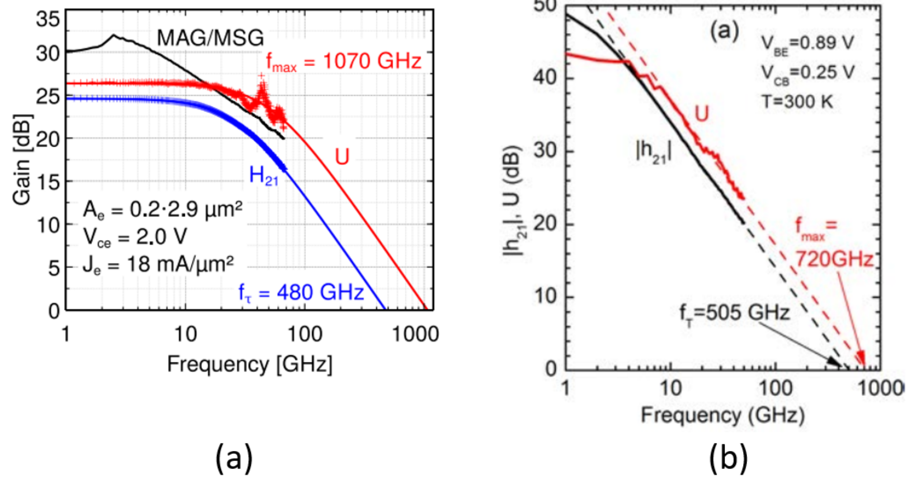


FIGURE 3.9: (a) Indium phosphide heterobipolar transistor technology f_{max} beyond 1 THz, [46]. (b) SiGe HBT with f_{max} of 720 GHz, [51].

verification of this model is shown in Fig. 3.11a. The model demonstrated a good agreement with predicted values of S-parameters for cryogenic conditions for two different bias: bias for peak of β (i.e. $J_C = 0.07\ mA/\mu m^2$), and bias for $J_C = 1\ mA/\mu m^2$. Fig. 3.11b,c shows both measured f_t and β as a function of collector current density, J_C. It is observed that the peaks occur at different values of J_C. In this sense, data from [41] shows that g_m at 15 K increases around 13 times its value from bias for peak of β (J_C around $0.1\ mA/\mu m^2$) to bias $J_C = 1\ mA/\mu m^2$, which is closer to peak for f_t. This is consistent with the expression of f_t for bipolar transistors, [41]:

$$f_t \approx \frac{g_m}{2\pi(C_{BE} + C_{CB})}, \tag{3.9}$$

which is proportional to g_m. In addition, the expression for f_{max} is shown bellow, [41]:

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi r_b C_{CB}}} \tag{3.10}$$

It can be noted that for a given collector current density, faster device operation is achieved at cryogenic temperatures than at room temperature. From Table 3.1, it is possible to observe that g_m increases its value around 3.5 times when achieveing 15 K with room temperatures, in contrast with f_t that does not increase on the same scale. This is because the base to emitter capacitance has increased by a factor of two, and it is believed that this increase in capacitance is due to the

increase in the device turn on voltage from ∼0.65 V at room temperature to ∼1 V at 15 K, [64].
For the noise performance analysis, the expression of noise measure is used, M, because it takes into consideration both the noise figure, F, as well as the exchangeable gain G_e, which is similar to the available gain, but is extended to devices that are potentially unstable, [64, 65]. The noise measure is the noise temperature of an infinite cascade of devices, T_{CAS}, normalized at $T_o = 290\ K$. Therefore, the cascaded noise temperature, T_{CAS}, is given by:

$$T_{CAS} = T_o M = T_o \frac{F-1}{1-1/G_e} = \frac{T_n}{1-1/G_e} \tag{3.11}$$

T_{CAS} has a fundamental property, its minimum value regarding source impedance, $T_{CAS,MIN}$, is invariant to any lossless network that embeds tge devices; that is, it is invariant to lossless input, output, and feedback networks. A lossy network can only increase $T_{CAS,MIN}$, [64]. Fig. 3.11d shows the $T_{CAS,MIN}$ for the modeled HBT at 15, 77, 200 and 300 K. By cooling the device from 300 to 15 K,$T_{CAS,MIN}$ improved its value in a factor of fifteen. This demonstrates the excellent noise performance of the SiGe HBTs, achieved in cryogenic temperature conditions.

T	r_e	r_b	r_c	g_m	g_{be}	C_{cb}	C_{be}	C_{cs}	τ_d	f_t	β
K	Ω	Ω	Ω	mS	mS	fF	fF	fF	pS	GHz	-
15	0.5	1.0	0.3	804	2.0	97	684	75	1.42	162	1400
300	0.7	1.8	1.9	224	1.1	96	306	60	0.17	79	266

TABLE 3.1: Data from [64]: Extracted parameters values at $J_C = 1\ mA/\mu m^2$ and $V_{CB} = 0.5\ V$ for 15 and 300 K.

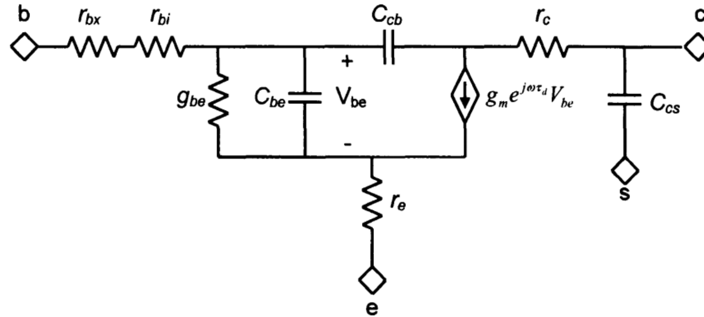


FIGURE 3.10: Small-signal equivalent circuit for SiGe HBT, [64].

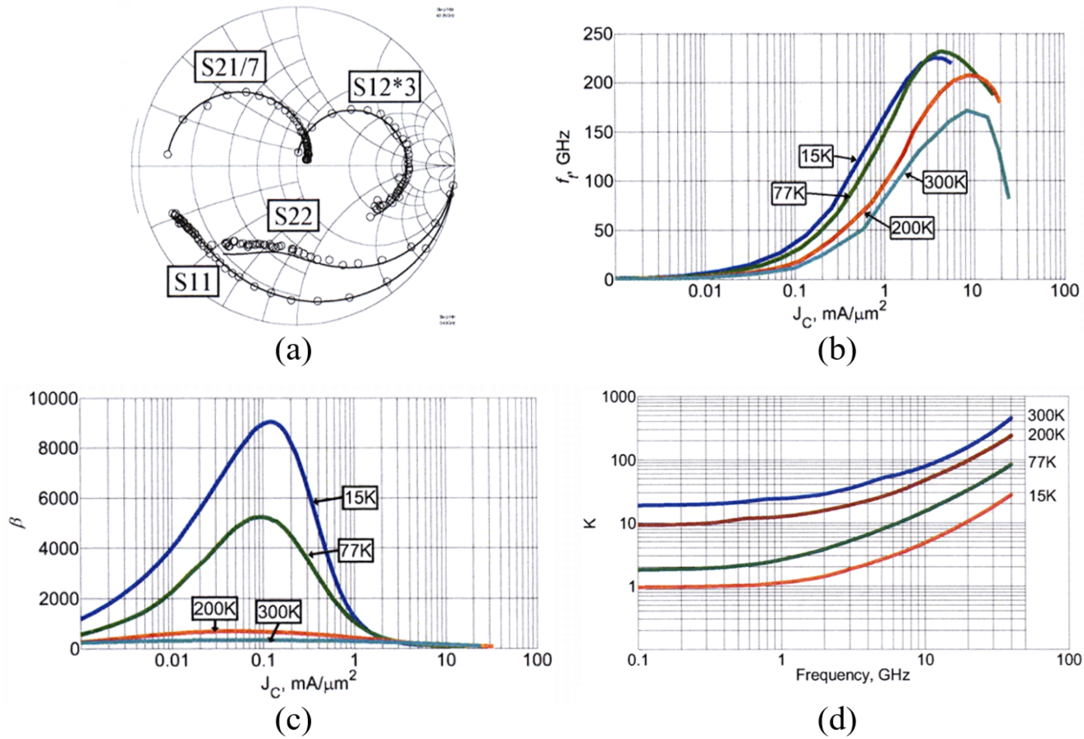


FIGURE 3.11: From [64]: Modeled (solid) and measured (circles) S-parameters at 15 K. Measured (b) f_t and (c) β as a function of J_C. (d) Minimum value of $T_{CAS,MIN}$ versus frequency at 15, 77, 200 and 300 K

3.2 Introduction to silicon-based technology for millimeter wave cryogenic receivers

Applications such as radio astronomy or remote sensing rely on cryogenic cooling systems to improve the sensitivity of their receivers. The state of the art in this type of receivers incorporates low-noise amplifiers (LNAs) developed using indium phosphide (InP) high-electron-mobility transistor (HEMT) technology, [2, 44, 55, 59]. This type of technology has historically dominated the field of extreme LNA, especially at cryogenic temperatures, [3, 4].
Silicon-based technologies, i.e. silicon-germanium (SiGe) heterojunction bipolar transistors (HBT) and CMOS transistors have demonstrated excellent RF performance, with the possibility of having a high integration of the functions in the same circuit, [5, 6, 77–82].
As seen in the previous section, the cryogenic models for both technologies have

already been developed showing a great agreement with the modeling and the measured, [64, 68]. Furthermore, SiGe has been shown to be able to operate them at temperatures as low as 70 mK, [66]. This has made SiGe HBT a competitive alternative to InP HEMTs for cryogenic RF LNA design.
The MMIC with HBTs operation at cryogenic temperatures has demonstrated a clear evolution in its operating frequency, as could be seen in Table 3.2. In this Table, it is also possible to see the good performance in power consumption. Along with its cryogenic operation, the silicon-based technologies have decreased their noise levels considerably. For instance, a SiGe amplifier, cryogenically cooled to 20 K, showed 95-116-K NT from 77 to 116 GHz, which means 6 to 7 times improvement in noise temperature compared to room temperature noise, [72]. However, despite improving their noise levels considerably, they are still not able to surpass the noise levels achieved with the InP technology. For example, in a band similar to the previous one (68-113 GHz), a InP LNA had NT of 25-36 K. CMOS technology has also improved its NT values in cryogenic conditions, achieving noise levels similars to those of the SiGe, see Table 3.2. It is worth mentioning that the amplifiers shown in Table 3.2 were designed with transistor models at room temperature, because there were no cryogenic transistor models available at the time of producing the designs.

Ref.	Temp. [K]	Bandwidth [GHz]	T_N [K]	Gain [dB]	P_{mW}
[67]	15	0.1-5	4.3*	> 29.6	20
[69]	19	0.5-4	< 8	> 25	8.3
[70]	15	19-23.5	≤ 45	> 20	< 0.9
This Work, [71]	20	52-65	191*	> 15.6	6.3
[72]	20	77-116	95-116	20	2.8
[86]	20	75-115	108-155	6-7.5**	22

Table 3.2: Comparison of the cryogenic noise performance of the state-of-the-art silicon-based LNAs.
*Average.
**Gain/stage.

InP/silicon-based hybrid solutions are presented with the aim of taking advantage of the excellent noise levels offered by the InP technology, combined with the high integration of functions for the silicon-based circuits. InP/CMOS hybrid solutions make it possible to obtain low-noise figures with lighter weight and possible lower power consumption. These systems utilize CMOS system-on-chip (SOC) with

presiding InP low-noise amplifier, [7]. In order to obtain high gain with low loss, horn antennas with waveguide packaged front-ends are used for these radiometers. Due to the conductor backplane and the fairly thin substrate, the packaging of GaAs or InP based MMICs is quite straightforward, [8]. However, the thick lossy silicon substrate with ground return current path on top of the substrate presents some challenges for waveguide packaging of CMOS or SiGe chips. As was one could see, the progress using silicon-based technology is very promising, but it is still necessary to continue working on them. For this reason, this thesis offers a contribution to the state of the art of this technology based on the proposed objectives.

4

Cryogenic operation of a millimeter-wave silicon germanium low-noise amplifier

This chapter presents all the tests that demonstrate the operation of a W-band SiGe LNA under 20-K cryogenic ambient conditions. The chapter begins by describing the LNA design, continues with the description of the cryogenic cooling system used; and then, the stability measurements to verify the correct operation of the amplifier at these cooling levels. S-parameters and noise measurements are presented at ambient and cryogenic temperatures. Measurements of the 1-dB output compression point (OP1dB) are also presented. Finally, the chapter is concluded by comparing the results obtained with those of the state of the art.

4.1 50-70 GHz silicon germanium low noise amplifier

The LNA was designed in IHP's 0.13 μm SiGe BiCMOS technology with f_t/f_{max} of 250/340 GHz. Simplified schematic and micrograph of the LNA are shown in Fig. 4.1. A one-stage amplifier was designed in differential cascode configuration with inductors as an output load. It should be mentioned that there was no cryogenic transistor model available at the time of the LNA design. Differential configuration was chosen because of our future aim of integrating the amplifier with a differential mixer. Furthermore, on-chip transformers are used to convert the differential mode to single-ended mode and to ease the on-wafer measurements in a 50-Ω environment. The simulated loss of one transformer is around 0.8 dB

at room temperature. Emitter degeneration was not used in the amplifier design in order not to decrease the gain of the single-stage cascode LNA. The device size for common emitter and common base are $AE = 6 \cdot (0.12 \cdot 0.14)\mu m^2$ and $AE = 6 \cdot (0.12 \cdot 0.08)\mu m^2$. Moreover, on-chip transformers are used to convert the differential mode to single-ended mode and to ease the on-wafer measurements in a 50-Ω environment. The input matching was designed to resonate out flip-chip bumps when connecting the amplifier to a PCB substrate. This will lead to a somewhat poor input match when the amplifier is measured on-wafer. The simulated loss of one transformer is around 0.8 dB at room temperature. The amplifier is biased using on-chip current mirrors.

FIGURE 4.1: *(left)* Simplified schematic of the LNA. The bias network is not shown for simplicity. *(right)* Micrograph of the LNA. The chip size is 620 um x 325 m including pads. From: [71].

4.2 Cryogenic probe system for microelectronic devices

The instrument used to decrease the physical temperature of the LNA under test to 20 Kelvin was a commercial cryogenic probe station: Nagase, model BCT-21MRFZ. With this instrument it is possible to take on-wafer measurements while the LNA is maintained at a physical temperature of 20 Kelvin. The cryogenic probe system used in this work is shown in Fig. 4.2. Fig. 4.3 shows each part of the cryogenic probe system. And the RF signal flow direction inside this cryogenic system is shown in Fig. 4.4.

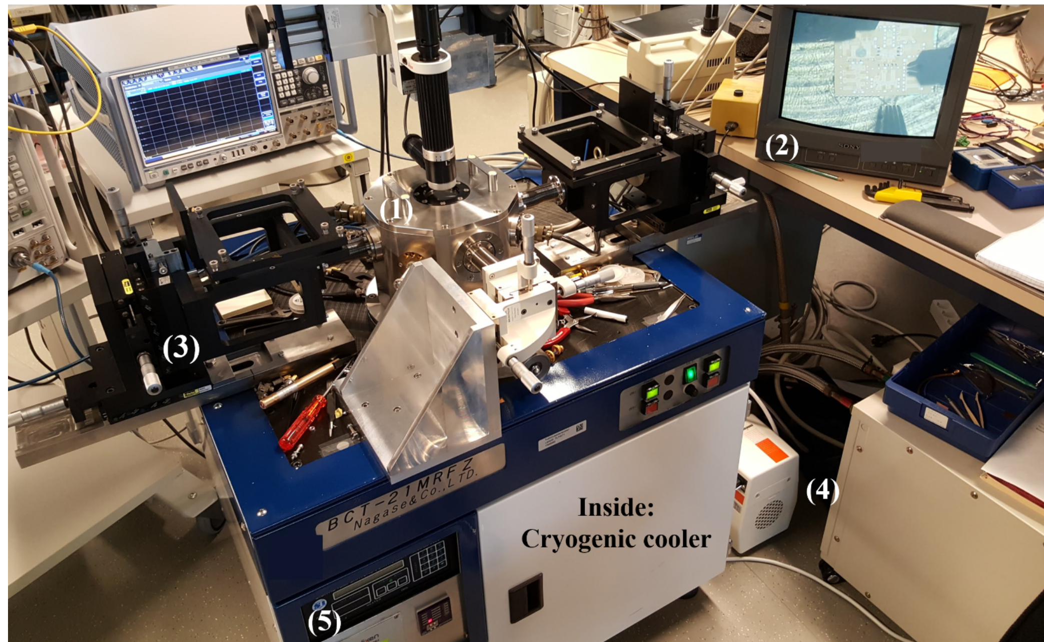


FIGURE 4.2: Cryogenic probe station for measurements of electronic devices at a temperature of 20 K. Nagase, model: BCT-21MRFZ. (1) Cryostat, (2) Screen for micro-chips visualization, (3) RF probe positioner, (4) vacuum pump and helium compressor and (5) digital temperature controller. From: MilliLab - VTT Technical Research Centre of Finland.

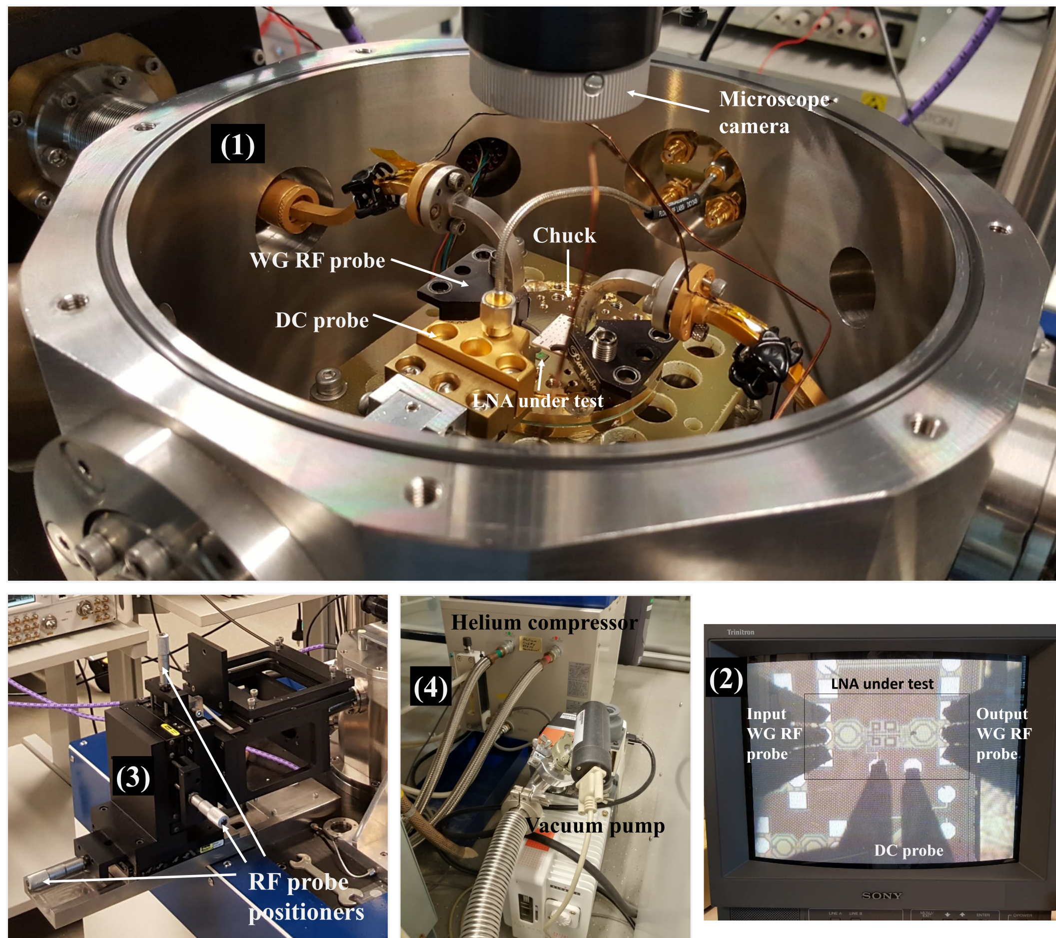
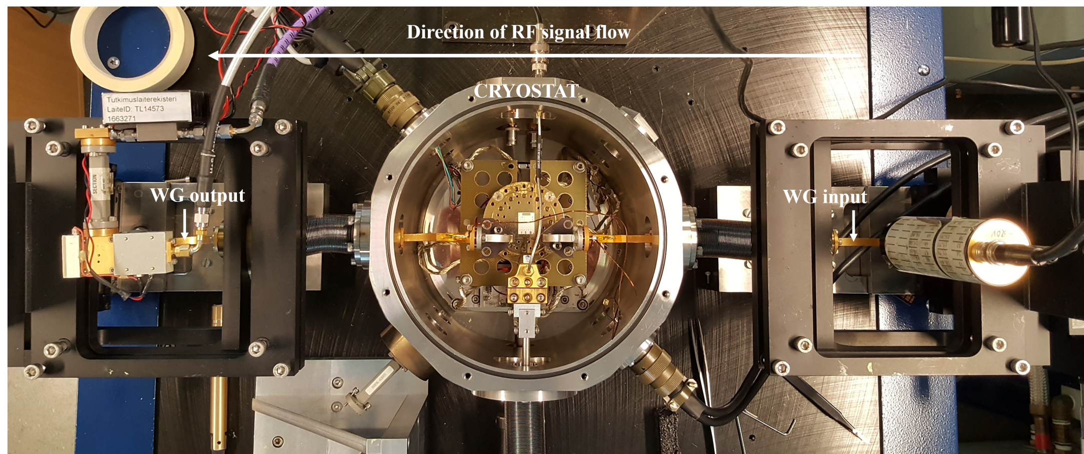


FIGURE 4.3: Parts of the cryogenic probe station system, image numbers came from Fig. 4.2. From: MilliLab - VTT Technical Research Centre of Finland.

4.3 Study of stability of the LNA

Changes in internal capacitances of the transistors at cryogenic conditions could modify the performance of the LNAs, exciting oscillations in the circuit. These oscillations appear at the output of the circuit in the form of undesirable narrowband power. The presence of the oscillations affects the noise and gain of the amplifiers. There are two experiments to perform the instability test: (1) measuring the output of the amplifier when a 50 Ω load is connected to the input. (2) Measuring the I/V curve of the amplifier. Both test were performed at a cryogenic temperature of 20 K.



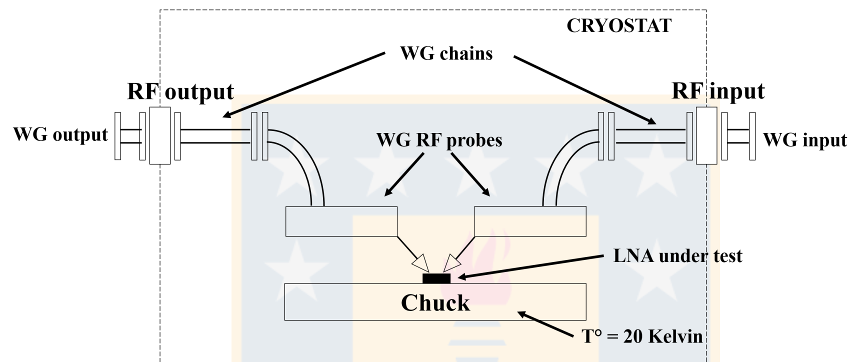


FIGURE 4.4: *(upper)*: Image of components that route the RF signal flow from the input to the output of the cryostat. From: MilliLab - VTT Technical Research Centre of Finland. *(lower)*: Diagram of the upper image.

4.3.1 Set-up for measuring the LNA output power at 20 K

This test is to verify if there are any peaks in the spectral content of the amplifier. If there are no peaks in the power spectrum of the amplifier, then the amplifier is not oscillating in the measured band of frequency. The measurement was performed using the spectrum analyzer Rohde & Schwarz that works from DC to 50 GHz frequency band. This instrument is directly connected to the RF output of the probe station, and the input probe was connected to a 50 Ω to avoid reflections from the input of the amplifier. A diagram and an image of the experimental set-up, are presented in Fig 4.5.

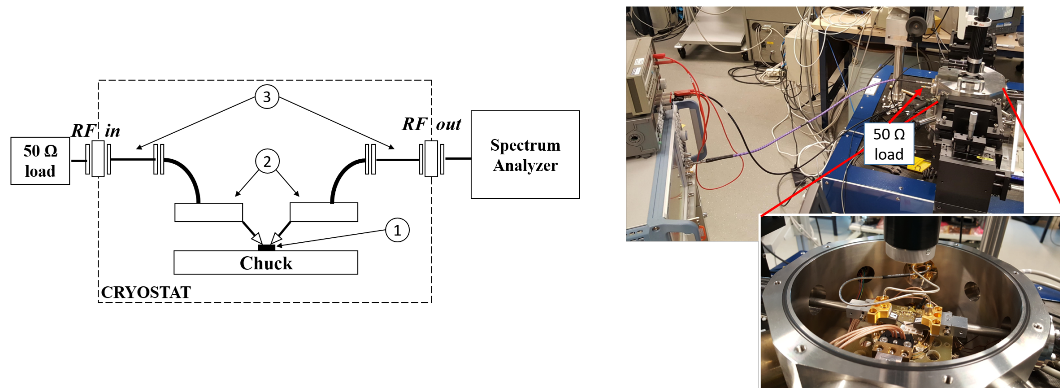


FIGURE 4.5: Diagram *(left)* and experimental *(right)* set-up for output power measurements of the amplifier. (1): Amplifier or device under test, (2) coaxial probes and (3) coaxial wires. From: MilliLab - VTT Technical Research Centre of Finland.

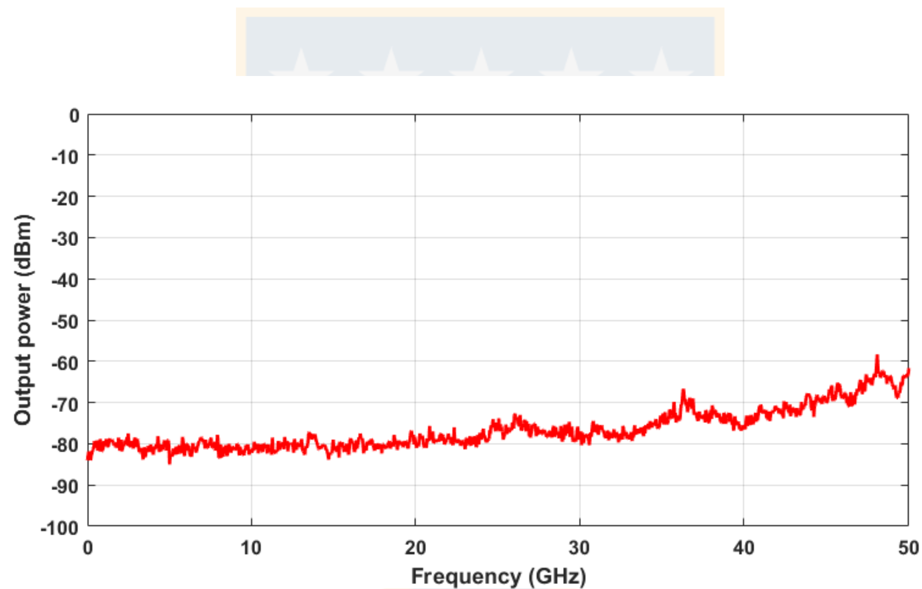


FIGURE 4.6: Output power spectrum of the amplifier from DC to 50 GHz, measured at 20 K.

4.3.2 Set-up for measuring the LNA I-V curves at 290 and 20 K

This test is performed to check that the I–V curve of the amplifier does not show sudden changes in the supply current at 20 K. These sudden changes could show the presence of oscillations in the circuit. The instrument used to perform this measurement was a precision semiconductor parameter analyzer: Agilent 4156C. This instrument can generate sweeps in the bias of the amplifier with a step of 5

mV. The input and output of the amplifier were connected to matched loads of 50 Ω. The bias of the amplifier is connected to the instrument used, and then the I–V curve is generated by sweeping the supply voltage with 5 mV steps, from 0 to 2.5 V.

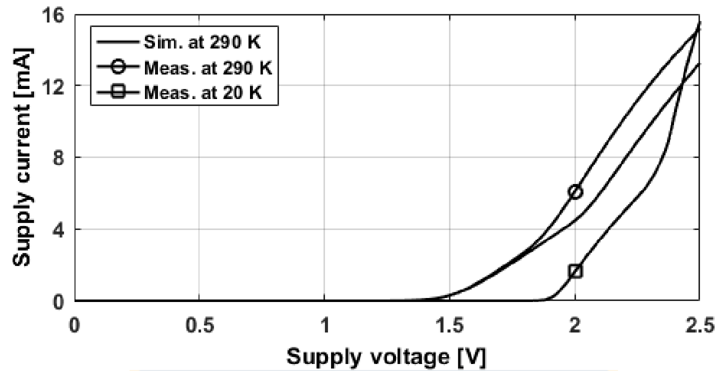


FIGURE 4.7: I-V characteristic curve of the amplifier at room temperature and cryogenic conditions, by sweeping the supply voltage in 5 mV steps.

4.3.3 Results and Analysis

The output power spectrum of the amplifier from DC to 50 GHz measured at 20 K is shown in Fig. 4.6, and the I–V curves for both temperature conditions are shown in Fig 4.7. The output power spectrum measurements at 20 K does not show signs of narrowband spikes, nor sudden changes in bias were observed at 20 and 290 K. Regarding the I–V curve measurements, this curve does not show sudden changes in the supply current at 20 and 290 K. In conclusion, both tests confirm the stability of the LNA at cryogenic conditions of 20 K and also at room temperature (290 K).

4.4 S-parameters of the LNA

Once it is determined that the amplifier has a stable operation at 20 K and of course at 290 K, it is possible to start with the characterization performance of the LNA. In this case, the characterization will be perform by measuring the S–parameters, noise figure and the derived gain from the noise figure measurements. In this section, the measurements of the S–parameters will be present at 20 and 290 K for a frequency band of 50–70 GHz. It is recommended to start with the

S–parameter characterization because it is possible to compare the behavior of the amplifier with its simulated S–parameter, in this case, at room temperature.

4.4.1 Set-up for measuring the S-parameters at 290 and 20 Kelvin

The experimental set–up used for testing the S–parameters is presented in Fig 4.8. To perform the S-parameter measurements, the samples are measured connecting the RF input and output of the cryostat to a vector network analyzer (VNA, HP, model 85109), using the access waveguides shown in Fig. 4.8. The system includes millimeter wave converters to extend the frequency range of the measurement setup to cover the range of interest. These converters can be represented by mixers in the diagrams. The VNA is calibrated inside the cryostat using on-wafer LRRM calibration [83].

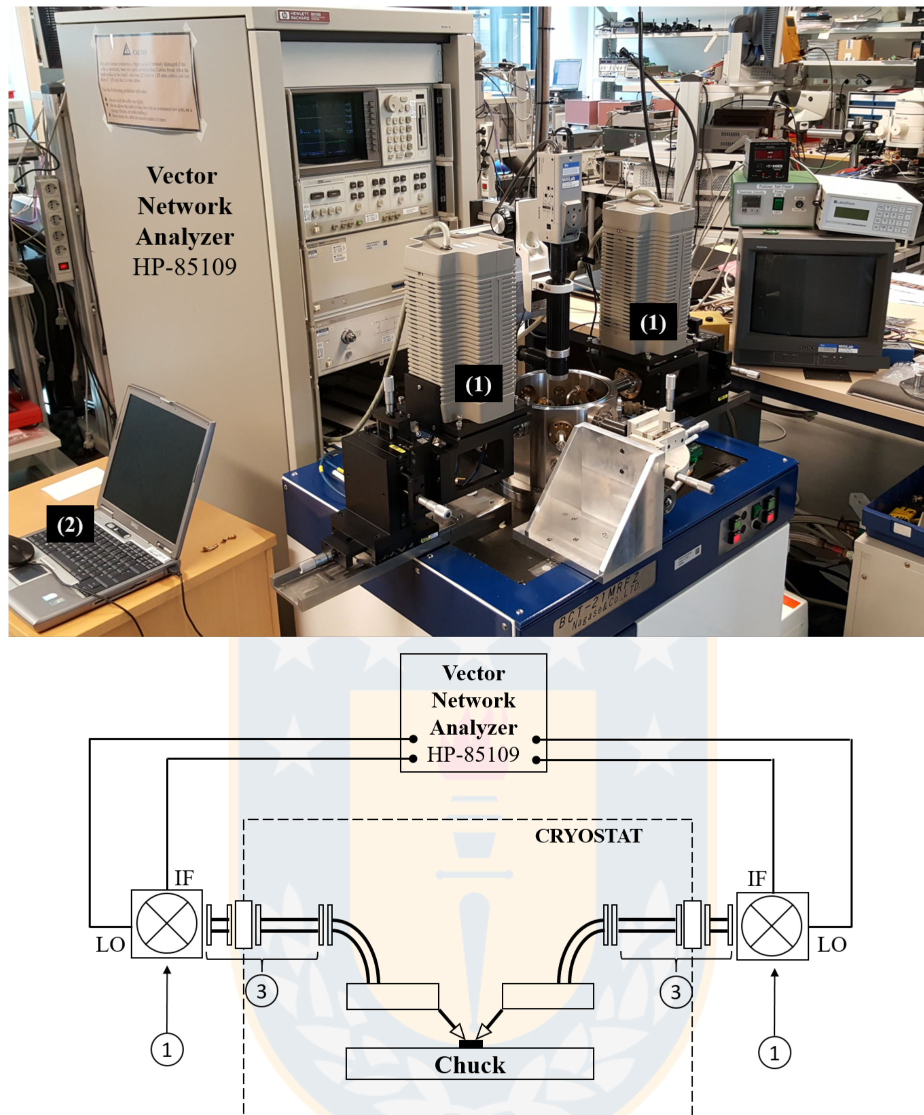


FIGURE 4.8: Image *(upper)* and diagram *(lower)* of the experimental set-up for S-parameter measurements in the 50-70 GHz band. (1) Millimeter wave converters for the VNA, (2) PC for data acquisition and the (3) access waveguides. From: MilliLab - VTT Technical Research Centre of Finland.

4.4.2 Results and analysis

Fig. 4.9 shows the S-parameters measured and simulated at room temperature and measured at 20 K. At room temperature, the measurements of the gain for a supply current of 5.5 mA reached a maximum value of 13.7 dB at 57.4 GHz. In general, the measured S-parameters are in fairly good agreement with the simulations. At 20 K, it is observed that gain reached a maximum value of 18.6 dB at 59 GHz, for a supply current of 3 mA (2.1 V supply voltage). The return losses have changed

compared with their values at room temperature. This is due to the fact that the transconductance of the transistor increases at cryogenic temperatures with a change in small-signal model associated capacitances and resistors as discussed in [64]. And also due to the possibility of a decrease in the supply current for low noise.

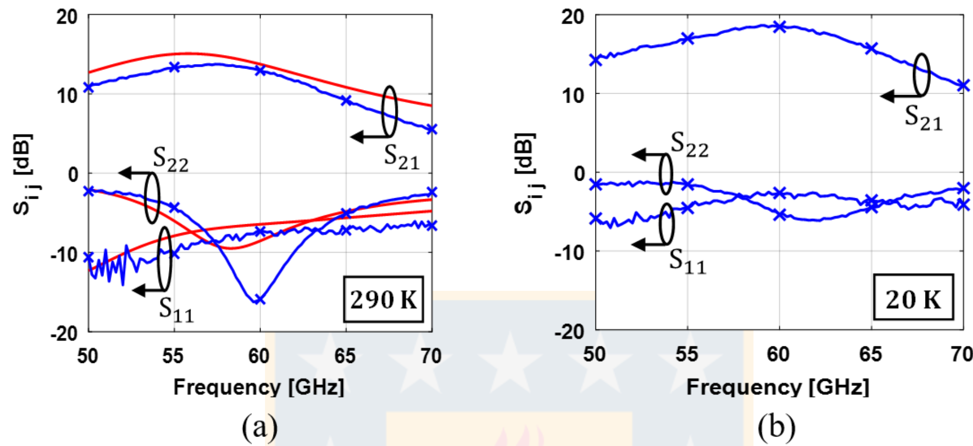


FIGURE 4.9: S-parameters of the amplifier. (a) Simulated (solid lines) and measured (solid lines with crosses) at 290 K. The bias point was 2 V @ 5.5 mA. (b) Measured at 20 K. The bias point was 2.1 V @ 3 mA. From: [71].

4.5 Noise and derived gain of the LNA

Fig. 2 shows a diagram with the component set-up internal to the cryostat. Set-up1 was used to perform automated NF measurements with a noise-diode, while Set-up2 was a verification set-up for measurements at 20 K using heatable load inside the cryostat as a noise source. In the Set-up1, the RF measurement signals are routed into the device under test (DUT), and out from the probe station through a pair of symmetric waveguides. The waveguides and the probe tips are not connected to the cryogenic cooling system. The noise diode (Millitech, model NSS-15-R1520) was used to provide the hot and cold temperatures involved in the Y-factor method. The excess noise ratio (ENR) of the noise source was previously measured in-house. In both set-ups, a down-converter block (DCB) was connected to provide intermediate frequencies (IFs) to the noise figure analyzer (NFA, Agilent, model N8973A). The calibration of the NF measurements was done as follows. The NF of the DCB was measured by connecting it directly to the noise diode and then routing its output directly to the NFA. The measured

value for the DCB was in the range of 4.4-6.5 dB over the 50-70 GHz band. The loss at temperature from the waveguides producing noise in the system is considered equal for both signal arms, including the waveguides and the probes. The loss of each arm, over the band of 50-70 GHz, was in the range of 1.7-2.7 dB at room temperature and 1.5-2.4 dB at 20 K. At both temperatures, the loss was measured using a 200 um long coplanar waveguide 'through' calibration standard to connect the input and output probes. The physical temperature of the probes was measured using sensors attached to them. In the case of Set-up2, the NF of the DCB was measured including the RF output probe plus waveguide, by means of the referred through standard. The measured NF for the DCB was in the range of 6.75-9.25 dB over the 50-70 GHz band, accounting for an input probe loss of 0.7 dB, and that both probes were connected to a second cooling stage of the cryogenic system to 50 K. The cold and hot temperatures for the heated load used in this set-up were 50 and 170 K, respectively. To obtain the TN of the DUT, the Y-factor method was used as shown in [84], and hence the noise derived gain extracted is obtained.

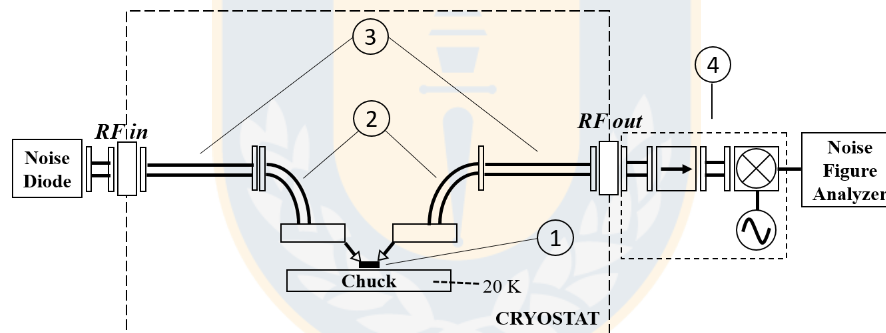


FIGURE 4.10: Diagram of the experimental set-up for noise figure measurements in the 50–70 GHz band, using a noise diode as a noise source outside the cryostat. (1): Amplifier or device under test, (2) WR–15 probes, (3) WR–15 waveguide set and (4) down–convertion block.

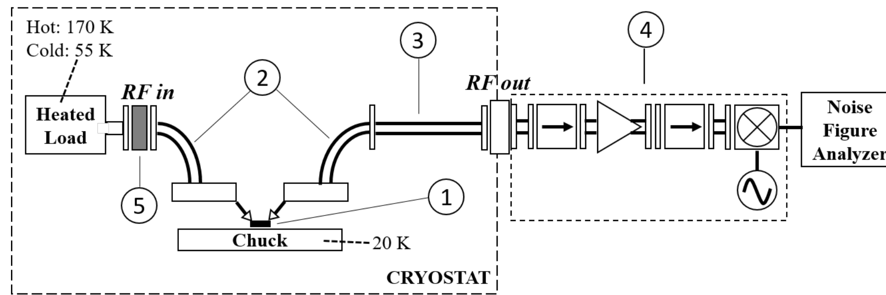


FIGURE 4.11: Diagram of the experimental set-up for noise figure measurements in the 50–70 GHz band, using a heatable load as a noise source inside the cryostat. (1): Amplifier or device under test, (2) WR–15 probes, (3) WR–15 waveguide set, (4) down–convertion block and (5) WR–15 thermal insulator.

4.5.1 Procedure to calculate noise and gain from noise measurements

The procedure used to calculate the noise and gain of the amplifier under test for both ambient and cryogenic temperatures is described below.

When the noise measurement was carried out, the system set-up shown in the diagram in Fig. 4.12 was used. This is composed of a noise source as the first element. Two of these were used to verify the results in this work: noise diode and heated load. Following the noise source, there is a set of waveguides and an input probe (WG1). Followed by the WG1, the LNA is connected, to which the gain and noise will be measured. The second set of waveguides and the output probe (WG2) are connected to the LNA as depicted in Fig. 4.12. The final part os the system is the back-end (BE), which is composed of a mixer and the noise figure analyzer. However, the BE components are assumed to be a single unit because we are not interested in measuring the noise of each of them.

In summary, we are interested in knowing the gain of the LNA (G_{LNA}) and its noise figure (F_{LNA}), therefore the Y-factor method will be used to determine them.

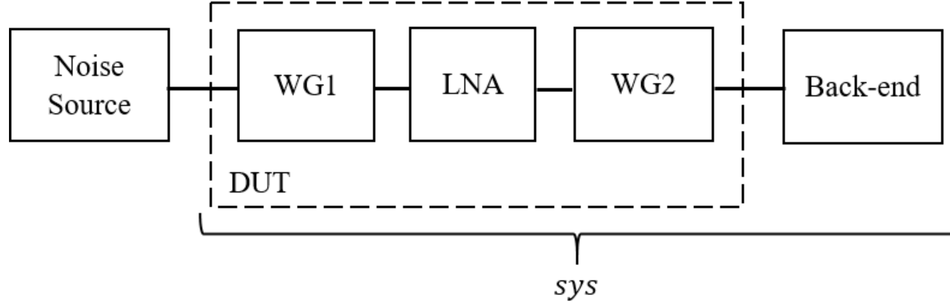


FIGURE 4.12: Chain of components for room and cryogenic measurements. The lines between boxes are for illustrative purposes only.

The first measurement performed is of the complete system (Fig. 4.12). The powers are measured at two different noise temperatures from the noise source. One temperature should be hot and the other cold.

$$P_{hot}^{sys} = KBG_{sys}(T_{hot} + T_{sys}) \tag{4.1}$$

$$P_{cold}^{sys} = KBG_{sys}(T_{cold} + T_{sys}) \tag{4.2}$$

Then, subtracting Ec. 4.2 from Ec. 4.3.

$$P_{hot}^{sys} - P_{cold}^{sys} = KBG_{sys}(T_{hot} - T_{cold}) \tag{4.3}$$

Rearranging, we find the relationship for KBG_{sys}.

$$KBG_{sys} = \frac{P_{hot}^{sys} - P_{cold}^{sys}}{T_{hot} - T_{cold}} \tag{4.4}$$

Then, it is known that the gain of the DUT, G_{DUT} is,

$$G_{DUT} = \frac{G_{sys}}{G_{BE}} = \frac{KBG_{sys}}{KBG_{BE}} \tag{4.5}$$

To find KPG_{BE}, it is necessary to take hot and cold measurements connecting only the BE to the noise source,

$$P_{hot}^{BE} = KBG_{BE}(T_{hot} + T_{BE}) \tag{4.6}$$

$$P_{cold}^{BE} = KBG_{BE}(T_{cold} + T_{BE}) \tag{4.7}$$

Then, subtracting Ec. 4.7 from Ec. 4.6 we found,

$$KBG_{BE} = \frac{P_{hot}^{BE} - P_{cold}^{BE}}{T_{hot} - T_{cold}} \tag{4.8}$$

So, replacing the Ecs. 4.4 and 4.19 in 4.5, we have,

$$G_{DUT} = \frac{P_{hot}^{sys} - P_{cold}^{sys}}{P_{hot}^{BE} - P_{cold}^{BE}} \tag{4.9}$$

In the above calculations it was assumed that T_{hot} y T_{cold} used in the Y-factor method measurement for the system and BE were equal. In case they were not equal, the expression for G_{DUT} equals to,

$$G_{DUT} = \frac{P_{hot}^{sys} - P_{cold}^{sys}}{P_{hot}^{BE} - P_{cold}^{BE}} \cdot \frac{T_{hot}^{BE} - T_{cold}^{BE}}{T_{hot}^{sys} - T_{cold}^{sys}} \tag{4.10}$$

Next, to find T_{DUT} the Friis equation (Ec. **??**) for T_{sys} was used:

$$T_{sys} = T_{DUT} + \frac{T_{BE}}{G_{DUT}} \tag{4.11}$$

To find T_{sys} and T_{BE}, the Y-factor method was used. We will start by finding T_{sys},

$$Y_{sys} = \frac{P_{hot}^{sys}}{P_{cold}^{sys}} \tag{4.12}$$

Then, T_{sys} is:

$$T_{sys} = \frac{T_{hot} - Y_{sys}T_{cold}}{Y_{sys} - 1} \tag{4.13}$$

Finding T_{BE} in the same way T_{sys} was found,

$$T_{BE} = \frac{T_{hot} - Y_{BE}T_{cold}}{Y_{BE} - 1} \tag{4.14}$$

Then, solving Eq. 4.13 we find T_{DUT},

$$T_{DUT} = T_{sys} - \frac{T_{BE}}{G_{DUT}} \tag{4.15}$$

As seen in Fig. 4.12, the DUT is made up of the chain of components: WG1, LNA and WG2. So, to find the gain of the amplifier (G_{LNA}), the Ec. 2.4 was used.

$$G_{DUT} = G_{WG1} \cdot G_{LNA} \cdot G_{WG2} \tag{4.16}$$

Solving it, we have that G_{LNA} is,

$$G_{LNA} = \frac{G_{DUT}}{G_{WG1} \cdot G_{WG2}} \tag{4.17}$$

To obtain G_{WG1} and G_{WG2} it is necessary to measure the system by removing the LNA and replacing it with a THRU transmission line. In practical terms, it is as if WG1 and WG2 were directly connected, i.e. it does not contribute to the electromagnetic performance. Fig. 4.13 is shows the set-up described above, and Fig. 4.14 shows two probes making contact using a THRU line.

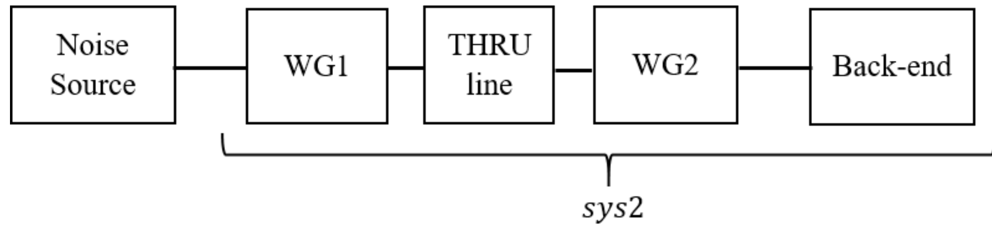


FIGURE 4.13: Chain of components for room and cryogenic measurements. The lines between boxes are for illustrative purposes only.

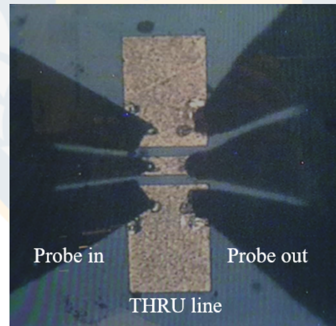


FIGURE 4.14: THRU line test.

For the system in Fig. 4.13 it is known that,

$$G_{sys2} = G_{WG1} \cdot G_{WG2} \cdot G_{BE} \tag{4.18}$$

G_{BE} is known from Eq. 4.19, and G_{sys2} is calculated as,

$$KBG_{sys2} = \frac{P_{hot}^{sys2} - P_{cold}^{sys2}}{T_{hot} - T_{cold}} \tag{4.19}$$

It is known that WG1 and WG2 are composed of exactly the same chain of components, and therefore, we can consider $G_{WG1} = G_{WG2}$. So, using Ec. 4.18 we have:

$$G_{WG1}^2 = \frac{G_{sys2}}{G_{BE}} \tag{4.20}$$

Thus,

$$G_{WG1} = G_{WG2} = \sqrt{\frac{G_{sys2}}{G_{BE}}} \tag{4.21}$$

Then, from Ec. 4.17 the G_{LNA} can be calculated.

For the calculation of F_{LNA}, the Friis equation (Ec. ??) will be used for the case of the NF:

$$F_{sys} = F_{WG1} + \frac{F_{LNA} - 1}{G_{WG1}} + \frac{F_{WG2} - 1}{G_{WG1}G_{LNA}} + \frac{F_{BE} - 1}{G_{WG1}G_{LNA}G_{WG2}} \tag{4.22}$$

To know the NF of WG1 (F_{WG1}), it is known that for a passive two-port network [10], we have to:

$$F_{WG1} = 1 + \frac{1 - G_{WG1}}{G_{WG1}} \cdot \frac{T_{phys}}{T_o} \tag{4.23}$$

Here, it was considered that $T_{phys} = 295K$ and $T_o = 290K$.

To know F_{sys} and F_{BE}, the NT of Eqs. 4.13 and 4.14 is converted, respectively, to NF using Eq. 2.2. Finally, from Eq. 4.22 we can solve F_{LNA},

$$F_{LNA} = G_{WG1}\left[F_{sys} - F_{WG1} - \frac{F_{WG2} - 1}{G_{WG1}G_{LNA}} - \frac{F_{BE} - 1}{G_{WG1}G_{LNA}G_{WG2}}\right] + 1 \tag{4.24}$$

4.5.2 Results and analysis

Fig. 4.15 shows the results at room temperature and 20 K for the NF and gain measurements, at 60 GHz, as a function of supply current. At room temperature, it is observed that the optimum bias point for NF starts around 6 mA and is maintained until 10 mA, with a nominal value close to 6 dB. At 20 K, it is observed that the optimum bias point for NF starts around 3 mA and is maintained until 10 mA. The nominal value for the NF in this range is approximately 1.8 dB, which can be explored with a dissipated power ranging from 6.3 mW to 24 mW.

The lower power operational regime is attractive for systems that require many amplifiers to operate, but have limited cooling capacity.

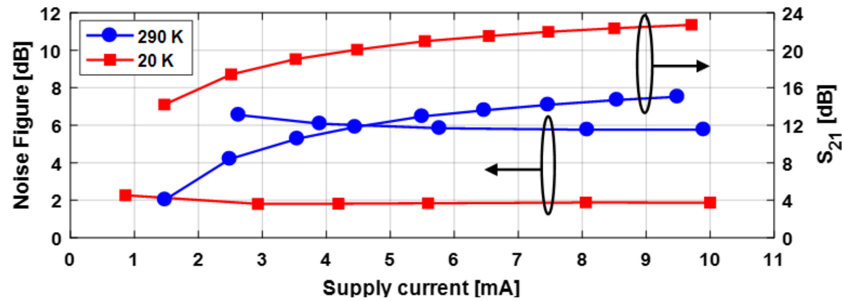


FIGURE 4.15: Measured noise figure (using set-up with noise diode, Fig. 4.10) and S_{21} at room temperature and 20 K for 60 GHz as a function of the supply current. The supply voltage was in the range of 1.7 to 2.47 V. From: [71].

The room temperature and 20 K measurements for NF and derived gain are shown together with the room temperature NF simulations, in Fig. 4.16. Over the measured frequency range at room temperature, and for a supply current of 5.77 mA, the DUT NF was in the range of 5.2-7.7 dB. At 20 K, the NF reached a minimum value of 1.4 dB at 59.5 GHz, for a supply current of 3 mA. As can be seen in Fig. 4.16a, the results of the NF measurements of the amplifier using both set-ups are consistent with each other.

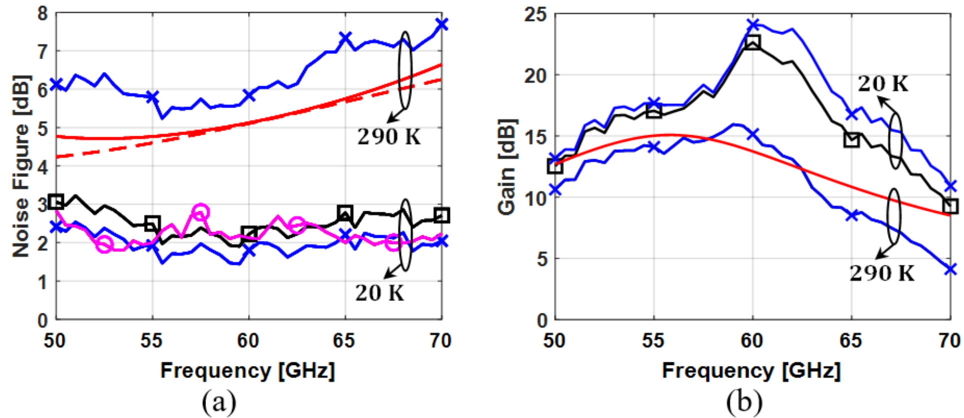


FIGURE 4.16: Fig. 5. Noise figure and derived gain of the amplifier at 290 and 20 K. (a) Noise figure. At 290 K: simulated (solid lined), simulated minimum NF (dashed line) and measured (solid line with crosses) using a noise diode as noise source. At 20 K: two samples measured using a noise diode as noise source (solid line with boxes and solid line with crosses), and one sample measured using a heated load as noise source (solid line with circles). (b) Derived gain. At 290 K: simulated (solid line) and measured (solid line with crosses). At 20 K: two samples measured using a noise diode as noise source (solid line with boxes and solid line with crosses). For both (a) and (b), the bias point used at 290 K was 2 V @ 5.77 mA and at 20 K was 2.1 V @ 3 mA. From: [71].

4.6 1-dB output compression point

To measure 1-dB output compression point of the amplifier, the set-up shown in Fig. 4.17 was used. This set-up started with a signal generator or synthesizer that provides signals up to 67 GHz, in this case a 60 GHz signal was used. Followed by this signal generator, an attenuator was connected to reduce the input power to the amplifier in order to generate the power gain curve from a low input power. Otherwise, the complete curve could not be generated because the amplifier would begin to compress, for example, in the first steps of input power. In Fig. 4.18 the measured curves of input power versus gain, and input power versus output power are shown. In this case the amplifier begins to compress at 16.2 dB of gain (or -10.7 dBm of output power), and it is possible to see that the gain is reduced by 1 dB when the output power is -1.42 dBm. In the case of the 20K cryogenic conditions, the OP1dB is -0.54 dBm.

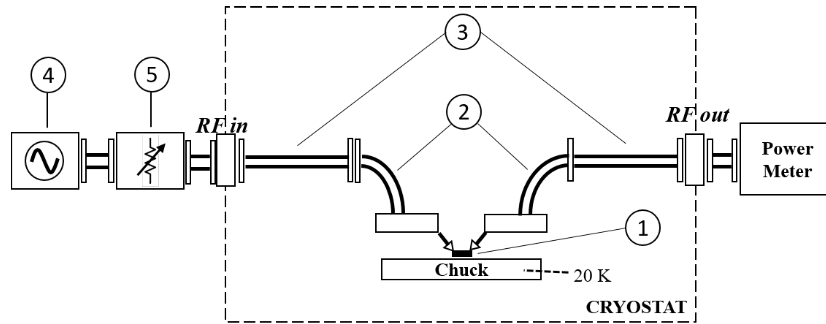


FIGURE 4.17: Diagram of the experimental set-up for 1-dB output compression point (OP1dB) 60 GHz frequency. (1): Amplifier or device under test, (2) WR-15 probes, (3) WR-15 waveguide set, (4) signal generator 67 GHz and (5) variable attenuator.

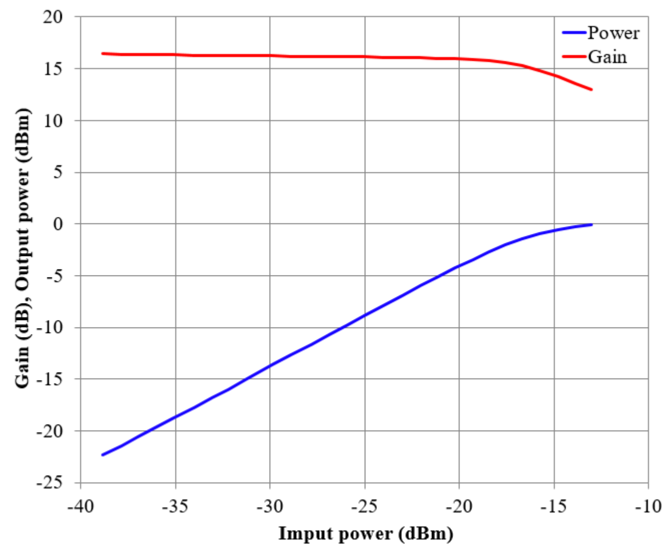


FIGURE 4.18: Measured curves of input power versus gain (red) and input power versus output power (blue) at room temperature.

4.7 Conclusion

In this chapter, the design and characterization of a SiGe LNA for the 50-70 GHz band was presented. We show, for the first time, the cryogenic performance for a SiGe LNA in this frequency range. The results of the amplifier characterization at 20 K are summarized in Table 3.2, and compared with the state of the art from the literature. When cryogenically cooled to 20 K, the amplifier reached an average NF of 2.2 dB (191 K) in the 52–65-GHz frequency band, this means that the T_N at 20 K ambient is 4.4 times less than at room temperature for the same frequency band. Finally, the amplifier consumed 6.3 mW at the optimal cryogenic

bias point, which is 1.8 times lower than at room temperature. According to the authors' knowledge, this is the lowest NF measured for a SiGe LNA in the 50-70 GHz band. The achieved NF is adequate for utilizing the amplifier as a second amplifier stage in a cryogenic radio astronomy receiver. However, future work is needed for optimizing the LNA performance using a cryogenic transistor model.

5 Package designs for a W-band silicon-germanium low-noise amplifier

In this chapter, the study for the packaging of a W-band SiGe LNA was carried out. In terms of electromagnetism, the devices needed to perform the packaging of this circuit are shown in Fig. 5.1. To make the design, simulation and optimization of the models presented here, the electromagnetic simulation software used was Ansys HFSS. Since the amplifier operates at a W-band, the whole system must work in this same frequency band. Therefore, for the design of the waveguides, these are considered equals by being from the same band. As mentioned in Chapter 2.3.2, the dimensions of the waveguides are standardized. In this case, the standard used is the WR-10, shown in Table 2.1. The recommended frequency for this standard is 75-110 GHz. For the design of the waveguige-to-microstrip transition, as the case of the waveguides, they are considered equals both for the input and for the output. The substrates used were: alumina ($\epsilon_r = 9.6$), AlN ($\epsilon_r = 8.8$) and megtron 7N ($\epsilon_r = 3.14$), [73]. These were selected according to the following criteria. Alumina was selected because it is widely available and is a low cost solution. AIN was selected because its CTE is lower than the alumina CTE, providing a better match for silicon, see Tabla 2.3. Megtron 7N was selected because of its dielectric properties, dielectric thickness availability and ease of processing. The multilayer PCB is constructed by sequential lamination processing. In the standard commercial PCB production, the minimum line, spacing and laser drill diameter are 50/50/90 μm, respectively, [75]. In [74, 75] presented excellent RF performance, showing a minimum of -1.2 dB at 110 GHz for a miscrostrip transmission line in the 110 to 170 GHz band. Furthermore, in this same

frequency band it presented a minimum of -1.8 dB at 110 GHz for a PCB-bumps set, [74].

S-parameters	Requirement
S_{21}, S_{12}	> 0.5 dB
S_{11}, S_{22}	< -15 dB

Table 5.1: Imposed requirements for probe design.

To make the design of the probe for both substrates, Table 2.2 was used, which is based on the dimensions presented in Fig. 2.20. The model #4 was selected, which is Alumina-100 (ϵ = 9.6), because it has a dielectric constant similar to the selected substrates. Then, models were tuned by modifying the dimensions WI, WT, WC, and LT. The tune was carried out based on the Smith chart and for matching the impedance to 50-Ω. WD was chosen by using TXLine tool (from AWR software) for a 50-Ω microstrip transmission line. The probe design with megtron 7N, used the same methodology as for alumina, but selecting the material #1, which is Teflon-127 (ϵ = 2.2). The requirements are imposed to be the S-parameters presented in Table 5.1.

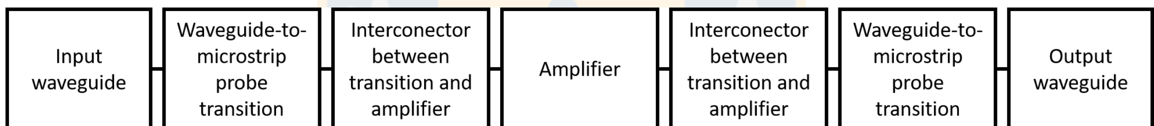


Figure 5.1: Chain of devices needed to make the packaging of the SiGe amplifier.

The interconnects to be used are of two types: wire-bonds and flip-chip. Wire-bond was selected because it is widely used and low cost, however, as shown in Section 2.3.3.1, at high frequencies they present high inductance. Flip-chip was selected because it has better high frequency performance than wire-bonds, as mentioned in Section2.3.3.2.

The SiGe LNA to be packaged was presented in 5.2, and it was designed in IHPs 0.13-μm SiGe BiCMOS technology with f_t and f_{max} of 350 and 450 GHz (at room temperature), respectively. Fig. 5.2 shows the micrograph and S-parameters. As it is shown in the figure, the pad pitch length is 150 μm, pads are in Ground-Signal-Ground configuration and the chip area is 1000 μm x 700 μm. Unfortunately, high pad capacitance effects are typical of this technology, [72].

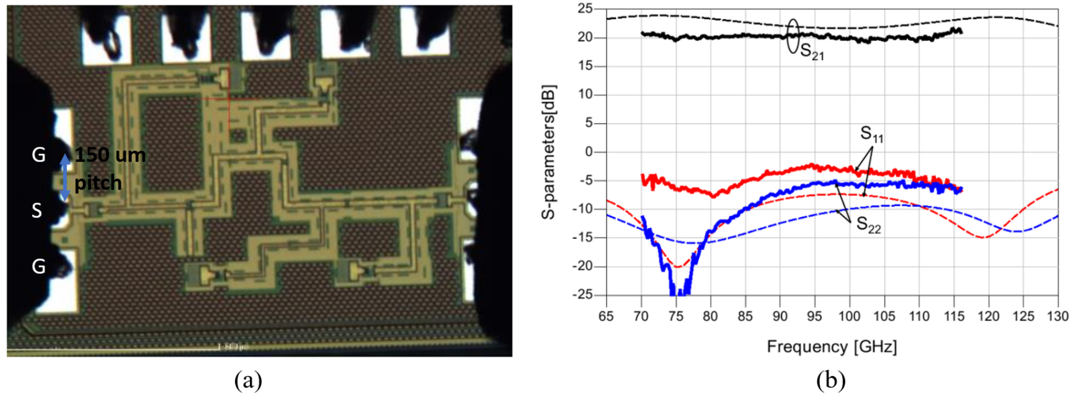


FIGURE 5.2: (a) Micrograph of the SiGe BiCMOS LNA for packaging. The chip size is 1000 μm x 700 μm including seal ring. (b) Measured (solid) and modeled (dashed) cryogenic (20-K) S-parameters of the LNA, [72].

Since the amplifier has a pad configuration of G-S-G, it is necessary to provide ground planes for the ground pads of the chip. For this reason, the microstrip line of the probe was transitioned to a coplanar line, in the same cases a linear tapering (see Fig. 5.3) was used, depending on the obtained performance of the probe. Based on Fig. 5.3 the dimensions of the WD2 and S were obtained using the TX-Line tool (from AWR software) for a 50-Ω coplanar transmission line. Minimum values for S are limited by the design regulations of the manufacture company Applied Thin-Film Products (ATP) from USA. The pitch of the coplanar transmission line is 150 μm (see Fig. 5.8), the same as the pitch of the SiGe LNA to be installed. The ground traces are connected by several vias to the ground of the motherboard, which rests in the block cavity. This is done to have a well-defined ground for the coplanar mode.

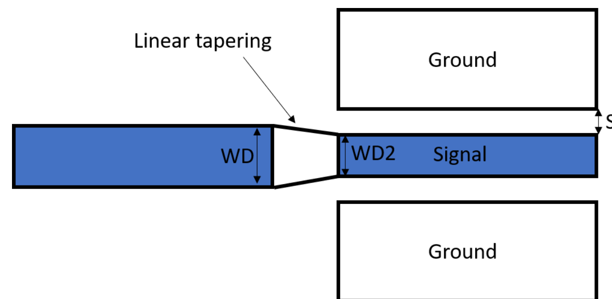


FIGURE 5.3: Microstrip-to-coplanar transition.

The HFSS simulations performed in this work for each waveguide-to-microstrip probe transition design are enumerated sequentially below:

1. Design of input probe without interconnect simulation, this is necessary to match the probe impedance to 50-Ω.
2. Design of input-and-output-probe (also called motherboard for flip-chip technique) with interconnect and pads of the SiGe chip, this is necessary for the next simulation.
3. Full system (Fig. 5.1) simulation, which is performed as shown in Fig. 5.4.

The full system simulation was carried out in AWR software, where each one of the devices of the chain (see Fig. 5.1) is connected. Therefore, the full system simulation can be done. To make this full simulation, it is necessary to de-embed the pads of the SiGe chip, because they are considered in the HFSS simulation (see 5.10). In this way, the effects introduced by the interconnects are also included. The de-embeding was performed in AWR. Fig. 5.4 shows the simulation set-up used for full system simulation in AWR.

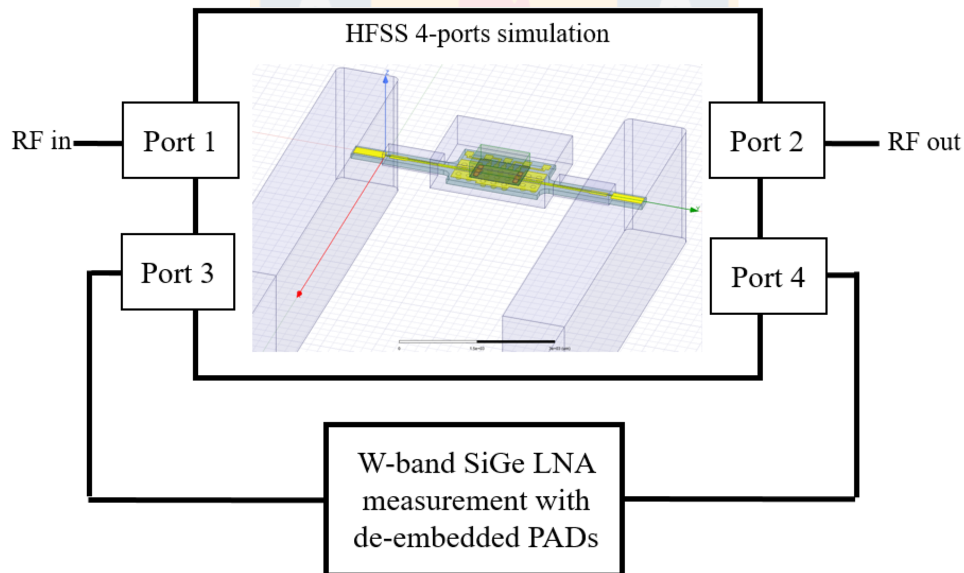


FIGURE 5.4: Full system simulation set-up used in AWR.

5.1 Probe designs using Alumina substrate for implementing wire-bond and flip-chip techniques

In this Section, two probes are presented for the implementation of wire-bond and flip-chip techniques.

5.1.1 Wire-bond

This probe was the only one that has not been designed in this work, because this probe was already designed by one of our collaborators, which is JPL. Therefore, the model of the probe was reproduced in this work. The dimensions of the probe are provided in Table 5.2. The reproduced model is shown in Fig. 5.5. The S-parameters for the full system are shown in Fig. 5.6. It is possible to observe that between 75 and 80 GHz S_{11} has the same behavior of the LNA, unlike S_{22} which obtains higher values. Between 80 and 105 GHz we see that the input and output impedances of the amplifier were matched in a better way than in the previous probes, achieving lower values than the reflections of the amplifier. Between 105 and 116 GHz the impedances become mismatched, since the S_{11} and S_{22} begin to exceed those of the LNA and reach 0 dB at 112 GHz and remain around this value until the end of the band. This is what it is expected for high frequencies using wire-bonds, due its high inductive effects. However, more matching can be performed.

Probe	ϵ_r	HC	HD	WC	WP	D	WI	LI	WT	LT	WD2	S
Alumina	9.8	254	101.6	460	200	600	50	100	130	350	54	53

TABLE 5.2: Reproduced dimensions of the Alumina probe for wire-bond technique. All units are in μm.

5.1.2 Flip-chip

This probe needs a microstrip-to-coplanar transition as it was mentioned in the introduction. However, no additional linear tapering was needed. The dimensions

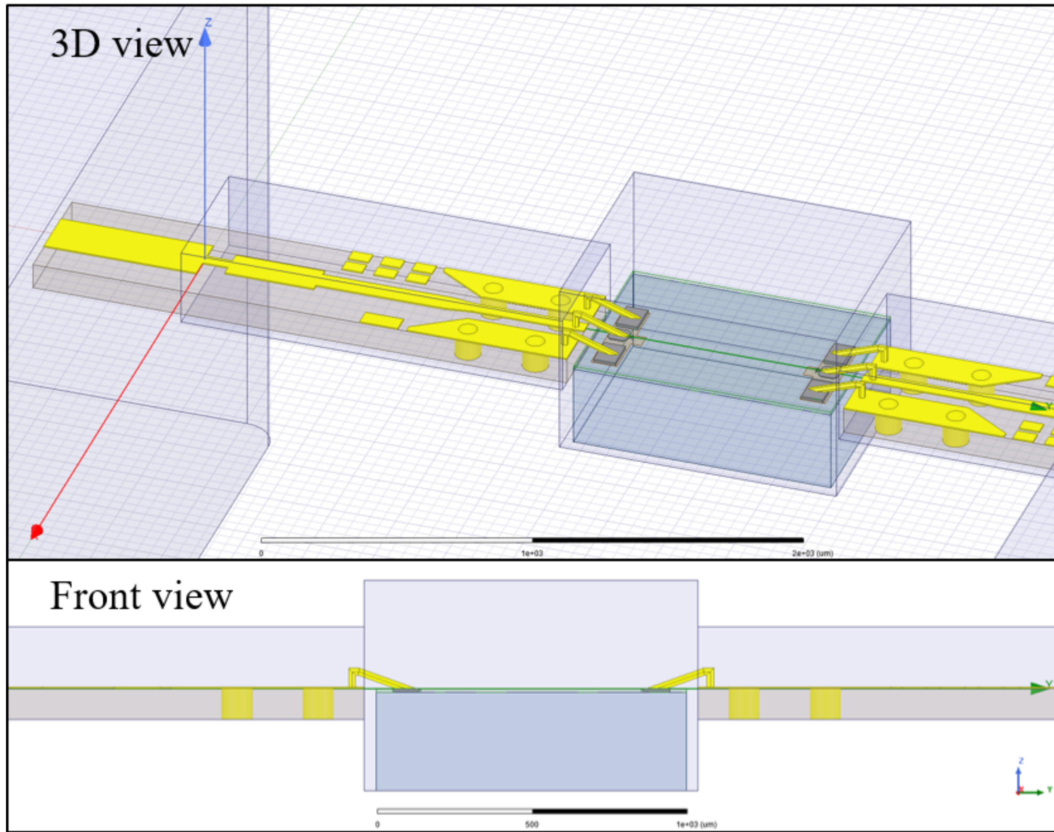


FIGURE 5.5: Full system model for Alumina probes with wire-bond technique.

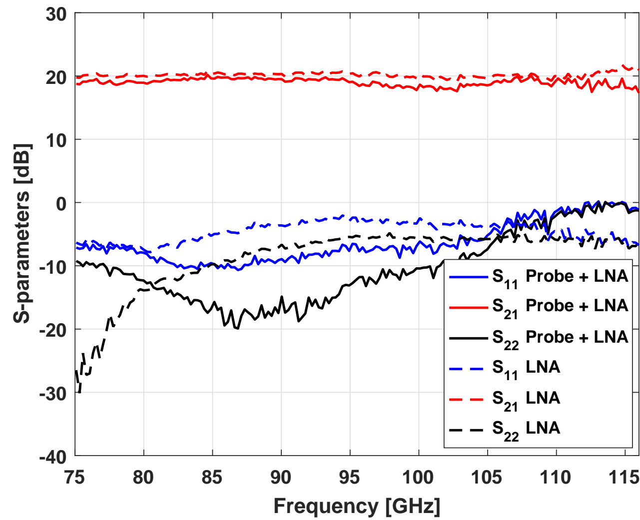


FIGURE 5.6: S-parameters of the full system of Fig. 5.5.

of the probe are provided in Table 5.3. The model is shown in Fig. 5.5. The S-parameters for the simulation of probe design without interconnect are shown in Fig. 5.6. It can be seen that the S_{21} parameter is close to zero fulfilling the

requirement imposed. The reflection parameters did not fulfill the requirements imposed around 87 and 105 GHz.

Probe	ϵ_r	HC	HD	WC	WP	D	WI	LI	WT	LT	WD2	S
Alumina	9.8	254	76.2	305	205	660	31	100	117	350	48	38

TABLE 5.3: Dimensions of the Alumina probe for flip-chip interconnect. All units are in μm.

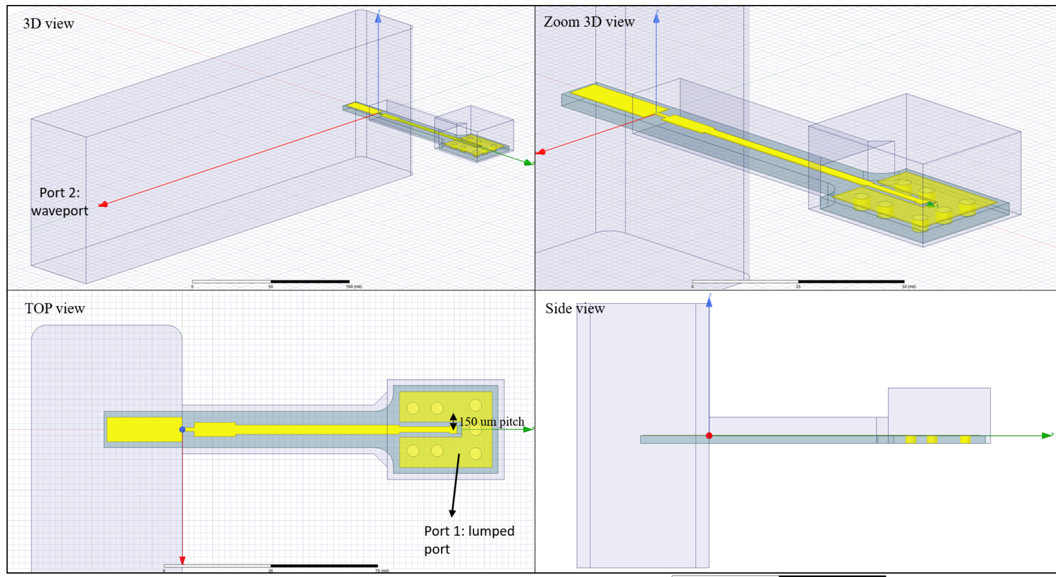


FIGURE 5.7: Alumina probe model for flip-chip interconnect.

The implementation of the input-and-output-probe is an extension of the previous model from the previous section, using two simple probes and joining them with several vias between them, to provide a well-defined ground at the end of the coplanar transmission lines. To model this probe, a silicon chip, (without integrated circuit) with the same dimensions as the SiGe amplifier, was placed at a distance from the motherboard for flip-chip, of 20 μm, which corresponds to the height of the bumps. This model is shown in Fig. 5.8. The final part of the coplanar transmission line is where the bumps will be connected to join the amplifier, see position of the bumps in Fig. 5.8. As can be observed in the figure, transmissions lines were installed for the DC connections of the amplifier, this means that the energization will be provided by an independent PCB. S-parameters for this design are shown in Fig. 5.9. S_{21} parameter meets the requirement across the band, reaching its best and lowest performance of -0.24 and -0.8 dB at 81 and 101 GHz, respectively. S_{11} parameter meets the requirement in most of the band, but

between 100 and 113 GHz it reaches a maximum value of -12.5 at 107 GHz. S_{22} parameter also meets the requirement in almost the entire band, however between 104 and 111 GHz, it reaches a value of -13.7 dB at 107 GHz.

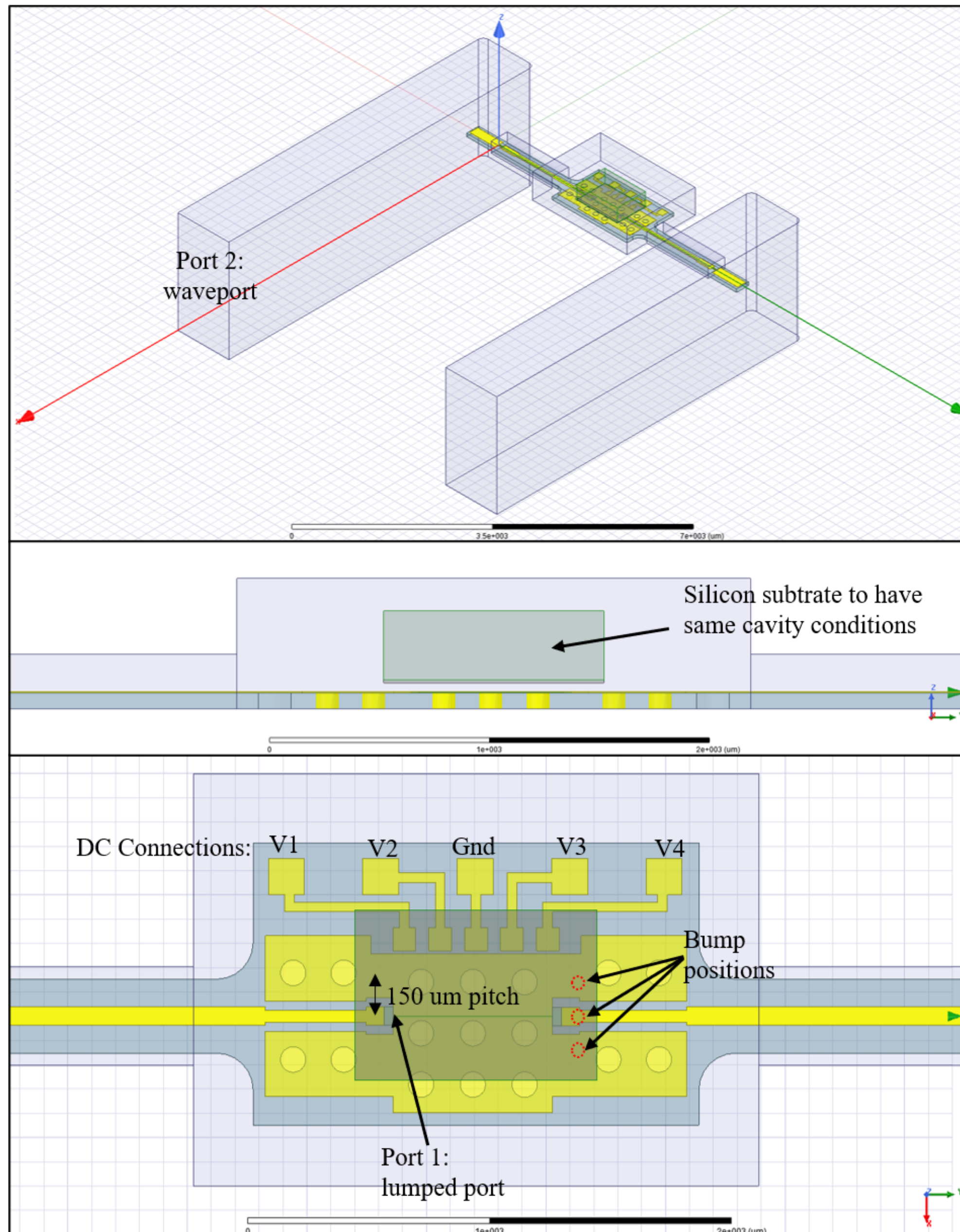


FIGURE 5.8: Design of input-and-output-probe (motherboard) Alumina probe for flip-chip technique.

Fig. shows the model to be used for the full system simulation. As was previously explained in the introduction, it is necessary to perform the de-embedding of the

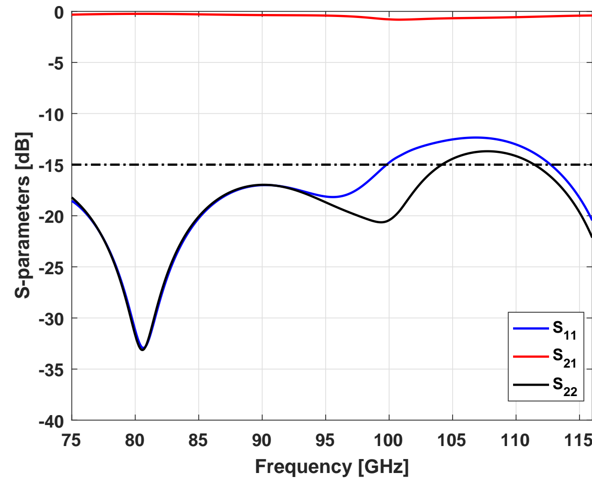


FIGURE 5.9: S-parameters for final Alumina probe design (Fig. 5.8).

pads, because the HFSS design already includes them, as shown in Fig. F. The S parameters of the full system simulation are shown in Fig. 5.11. S_{21} reaches its minimum value of 16 dB at 83 GHz. In general, over 90 GHz S_{21} reamins relatively close to the amplifier's value, reaching a maximum value of 19.7 dB at 107 GHz. Under 90 GHz, it separates the curve of the amplifier presenting a minimum of 16 dB at 83 GHz. In general, the return losses remain constant over 80 GHz in a value of around -5dB, achieving a slight improvement by the end of the band.

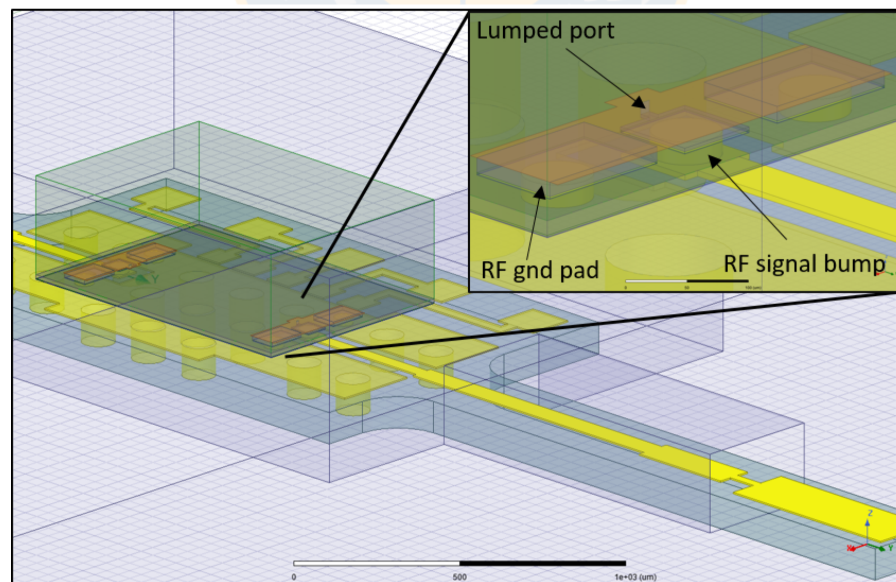


FIGURE 5.10: Final Alumina probe model considering the SiGe PADs and bumps for flip-chip technique. This model is for the full system simulation.

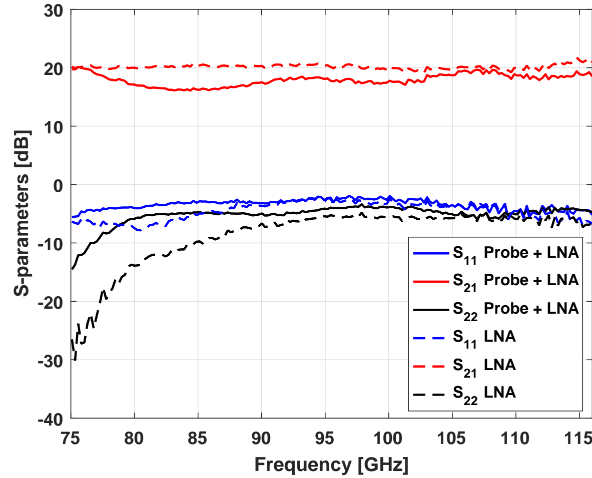


FIGURE 5.11: S-parameters of the full system simulation using alumina probe for flip-chip technique.

5.1.3 Comparison between wire-bond and flip-chip interconnects using Alumina substrate

The simulations for the interconnections by wire-bond presented a better performance at lower frequencies in the 75-110 GHz band as was expected, and they started to degrade their reflection performance at over 105 GHz and achieving 0 dB over 112 GHz. The flip-chip interconnection showed a better performance than the wire-bond in the same frequency band, maintaining the reflections nearly constant at around -5 dB up to the 105 GHz, where it starts to improve achieving a level of -7 dB in the 115 GHz. Based on the obtained S-parameters, it is possible to establish that the flip-chip interconnectors are more adequate for high frequencies. However, the possibility of manufacturing interconnects using wire-bond is not dimissed, because it is possible to use this technology at frequencies lower than the upper part of the band. For the following models, only the flip-chip interconnectors will be considered, given its good performance in the entire frequency range. It is worth mentioning that, a better impedance adaptaction was difficult to obtain, because the probe was designed for an environment of 50-Ω, but the SiGe amplifier presents a capcitive effect due to its pads. The latter is typical of this technology, [72]. In future designs, it is recommended to have a good coordination between the MMIC designer and the packaging designer.

5.2 Probe designs using aluminium nitride substrate for implementing flip-chip technique

The aluminium nitride (AlN), as mentioned in the introduction, was selected for having a CTE that adapts better than the alumina to the silicon's CTE, see Table 2.3. The design of the probe is very similar to the design of the alumina probe, which is why its 3D models were not shown as the previous cases. If it is important to see it, please refer to Fig. 5.8 and to see the full system simulation see Fig. 5.10. The similarity in the design is due to the dielectric constant of both materials is very similar too, therefore, the designs will be similar as well. Table 5.4 shows the physical dimensions of the design of the probe using AIN. The S-parameters are shown in la Fig. 5.12. S_{21} parameter meets the requirement in the entire band being within the margin of -0.24 and -0.44 dB. S_{11} and S_{22} parameters have very similar performances and meet the requirement in almost the entire band. Between 86 and 89 GHz, they reach a value of around -14.5 dB, and between 102 and 108.5 GHz they reach a value of -14 dB.

Probe	ϵ_r	HC	HD	WC	WP	D	WI	LI	WT	LT	WD2	S
Alumina	9.8	254	101.6	305	205	660	31	100	117	350	48	38

TABLE 5.4: Dimensions of the AlN probe for flip-chip interconnect. All units are in μm.

Fig. 5.13 shows the S-parameters of the full system simulation. In general, it shows a good agreement between the amplifier and the whole system, specially at over 87 GHz. Under 87 GHz, S_{21} has a minimum of 17.5 dB, S_{11}, and S_{22} presents a value of -4 and -7.7 dB, respectively.

5.3 Probe designs using megtron 7N substrate for implementing flip-chip technique

Megtron 7N was selected for its excellent RF performance, along with the benefits that the commercial processes offer (see ethe introduction of the chapter). The dimensions of the probe are provided in Table 5.5. The probe model using Megtron 7N prepreg is shown in Fig. 5.14. A difference with respect to the previous models

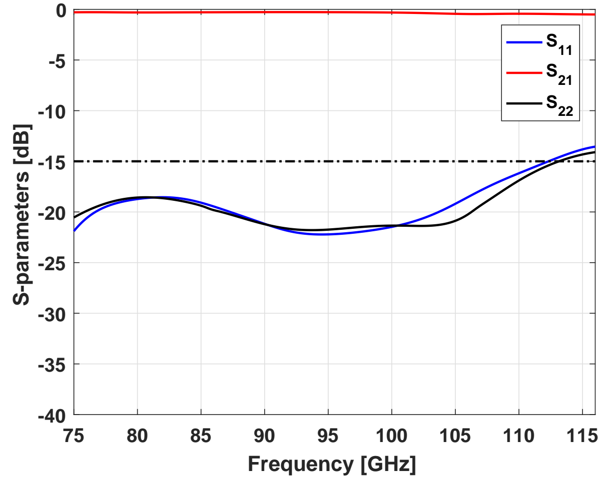


FIGURE 5.12: S-parameters for final AlN probe design (Fig. 5.8).

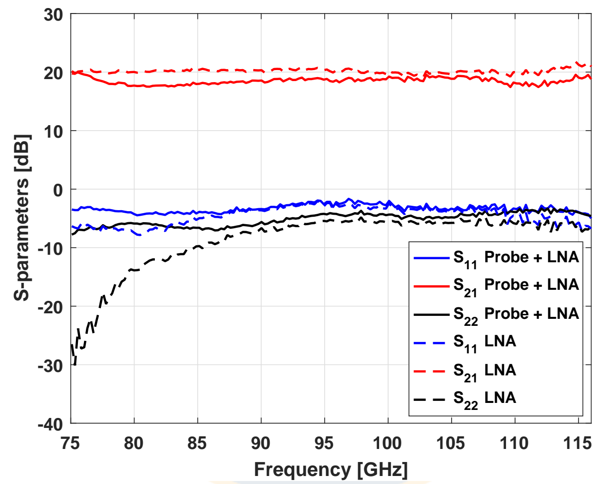


FIGURE 5.13: S-parameters of the full system simulation using AlN probe for flip-chip technique

is that this substrate needs another support substrate as the first layer underneath the entire probe designed. This can be seen in the side view of Fig. 5.14. As can be noted, the first layer has several vias so that the second layer has a well-defined ground, as if the second layer rested on the block itself. The name of the first layer material is Megtron 7N core and it has a dielectric constant of 3.3. The thickness of this first layer is of 127 μm. Fig. 5.15 shows the S-parameters of the designed probe. We can see the S_{21} parameter is very close to zero, fulfilling the requirement. Reflection parameters are very similar and also meet the requirement. S_{11} takes its minimum value at 83 GHz of -26 dB and its maximum value of -18 dB at 100

GHz.

Probe	ϵ_r	HC	HD	WC	WP	D	WI	LI	WT	LT	WD2	S
Alumina	9.8	407	79	305	205	660	50	100	110	350	50	50

TABLE 5.5: Dimensions of the megtron 7N probe for flip-chip interconnect. All units are in μm.

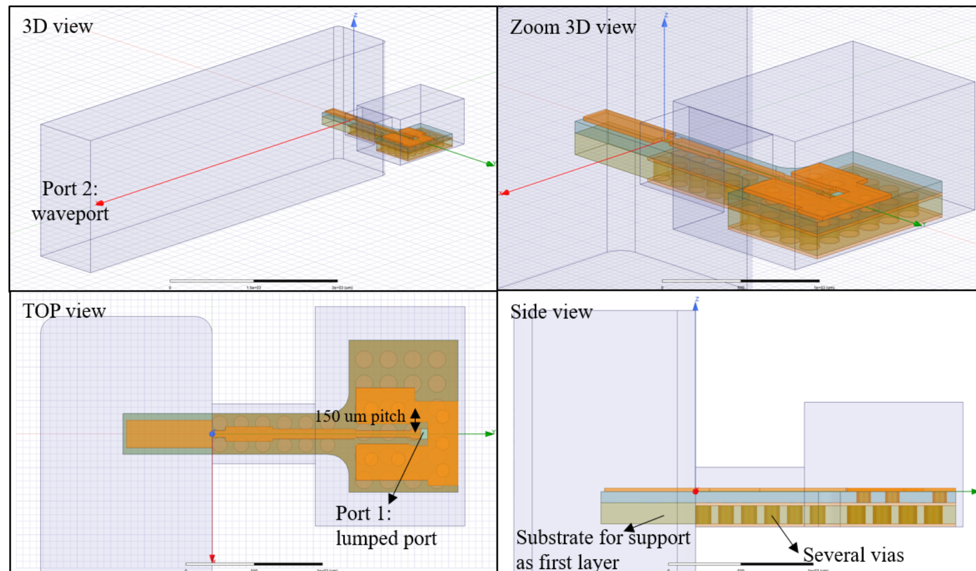


FIGURE 5.14: Megtron 7N probe model for flip-chip interconnect.

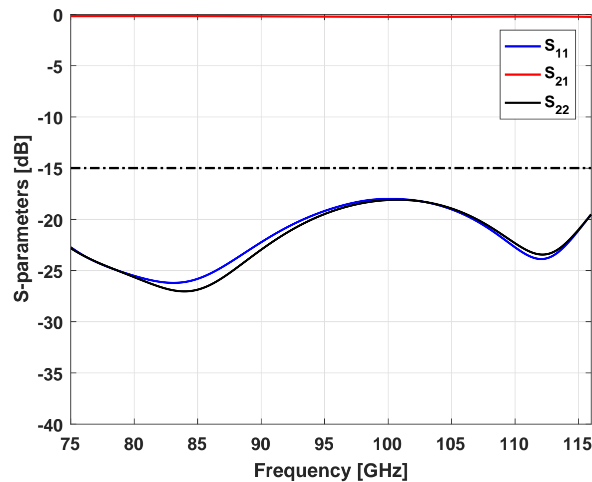


FIGURE 5.15: S-parameters for megtron 7N probe model for flip-chip interconnect.

Fig. 5.16 shows the model that will be used for the full system simulation. As was mentioned in the introduction, the de-embedding of the pads must be performed,

because as is shown in Fig. 5.10, the HFSS design already includes them. Fig. 5.17 shows the S-parameters of the designed probe. The electromagnetic behavior of the probe does not vary much with respect to the simple probe, showing similar S-parameters. The transmission parameter deviates a bit from 0 dB, but it is still very close, reaching a minimum of -0.28 dB at 102 GHz. The reflection parameters remain below the requirement, even below -19 dB. The global minimum is -34 dB and reaches it at 114 GHz.

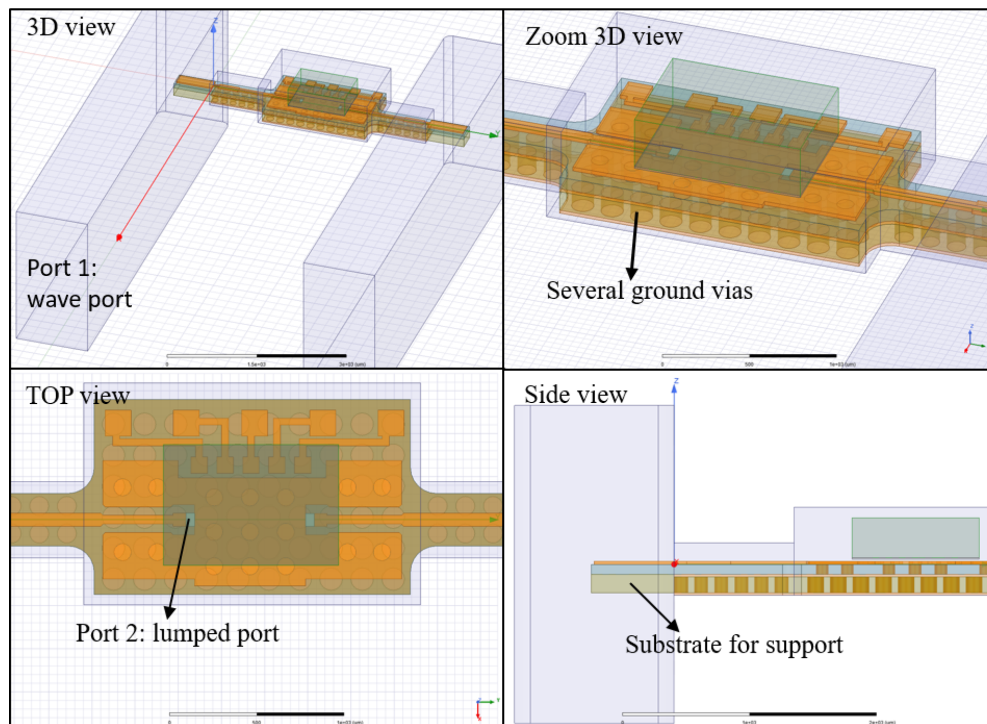


FIGURE 5.16: Design of input-and-output-probe (motherboard) megtron 7N probe for flip-chip technique.

Megtron 7N is a material from the commercial industry for the manufacturing of PCBs, so it is possible to manufacture the RF probes and DC circuit for RF filtering on the same PCB. This avoids the use of cables to provide the DC signals to the LNA. Here is a model that includes both the RF stage as well as the DC stage. Fig. 5.18 shows the layout of this PCB. As can be seen, the waveguides have a bending so that they can receive and expel the RF signal at the time of manufacturing the packing block, see Fig. 5.20. The complete system simulation (as in Fig. 5.4) was performed. The S-parameters of the complete system are shown in Fig. 5.19. As can be seen, the S_{21} parameter between 89 to 113 GHz shows a relatively constant behavior around 17.5 dB. Under 89 GHz it reaches a maximum of 19.9 dB at 77.8 GHz, and over 113 GHz a maximum of 20.2 dB at

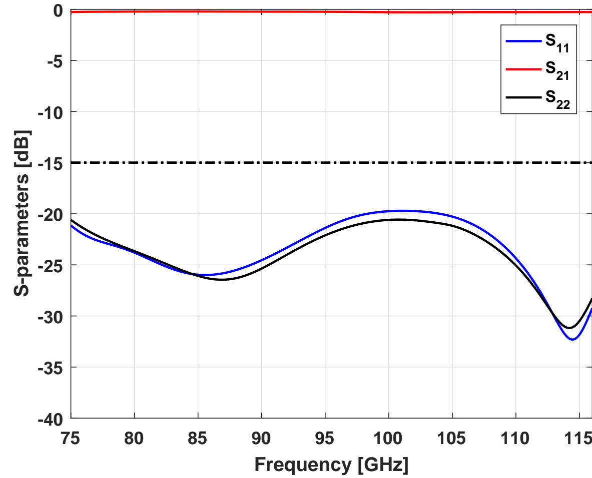


FIGURE 5.17: S-parameters for final megtron 7N probe design (Fig. 5.8).

116 GHz. S_{11} and S_{22}, in general, are consistent with the behavior of the LNA between 90 and 116 GHz. Under 90 GHz, S_{11} reaches its maximum of -1.9 dB at 84.5 GHz, and its minimum of -5.7 dB at 75 GHz. S_{22} reaches its maximum of -5 dB at 82 GHz, and its minimum of -14 dB at 75 GHz.
Finally, Fig. 5.20 shows the 3D modeling of the waveguide block for packaging the PCB together with the SiGe LNA in flip-chip mode. This block considers all the measurements that will be used for its manufacturing. The dimensions of the internal cavities were the result of the simulations shown earlier in this section. The external dimensions, such as screw threads, alignment pins and block slots, were designed so that the block had the smallest physical dimensions.

5.4 Conclusion

Three probe designs for flip-chip mounting of a silicon amplifier were proposed. They used alumina, AlN, and megtron 7N prepreg as substrates, respectively. Simulation of S-parameters including LNA measurements were presented. AlN and megtron 7N prepreg probes demonstrated the best transmission performance in the 75-116 GHz band. The S_{21}-parameter range of AlN and megtron 7N prepreg was 17.6-19.9 dB and 19.8-16.4 dB, respectively. Megtron 7N prepreg has advantages over AlN, which are the integration of RF probes, and the DC circuit on the

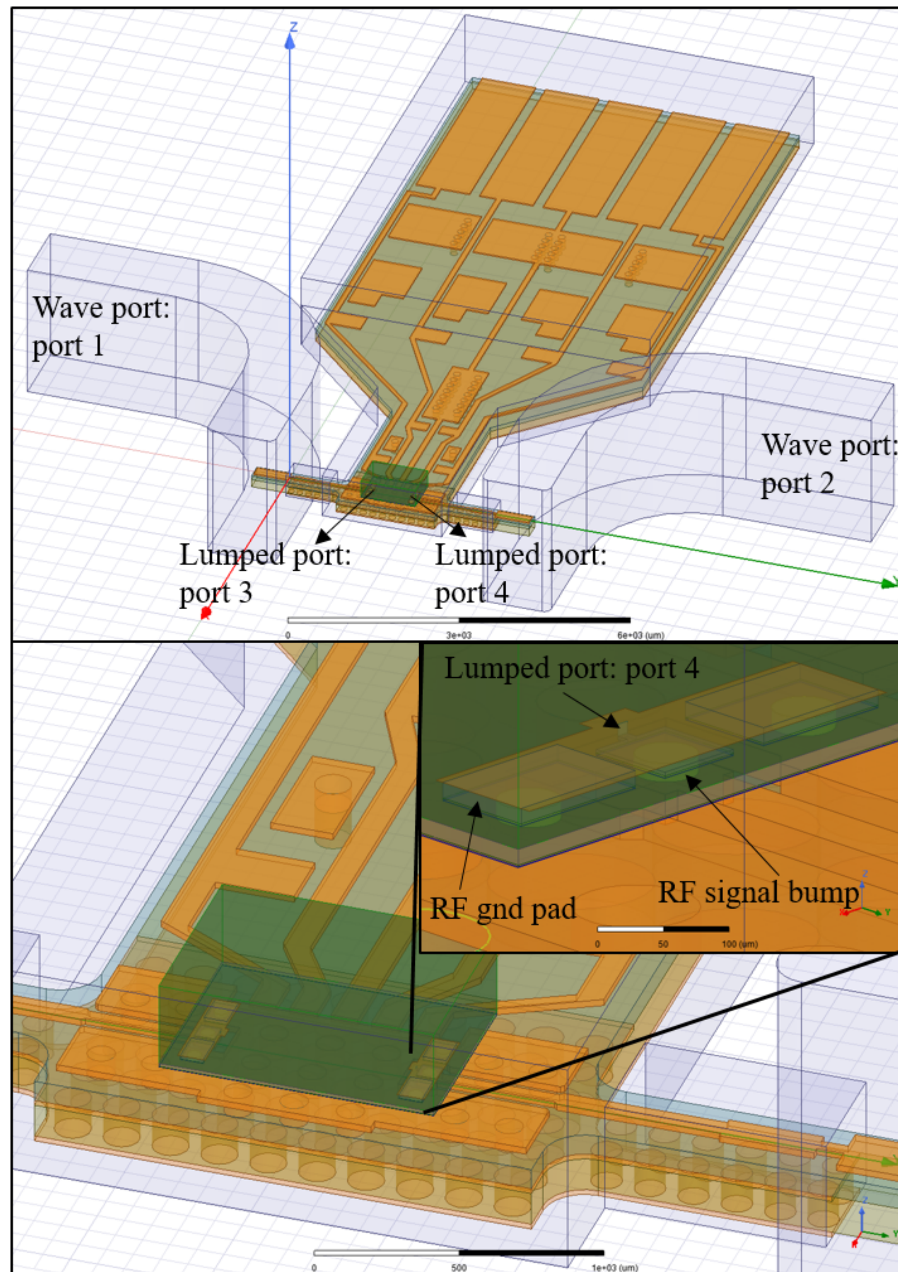


FIGURE 5.18: Final model of alumina probe considering the SiGe PADs and bumps for flip-chip technique. The probe design including DC circuitry on the same PCB within the final cavity of the model. This model is for full system simulation.

same PCB. A 3D solid block model of waveguides was proposed.

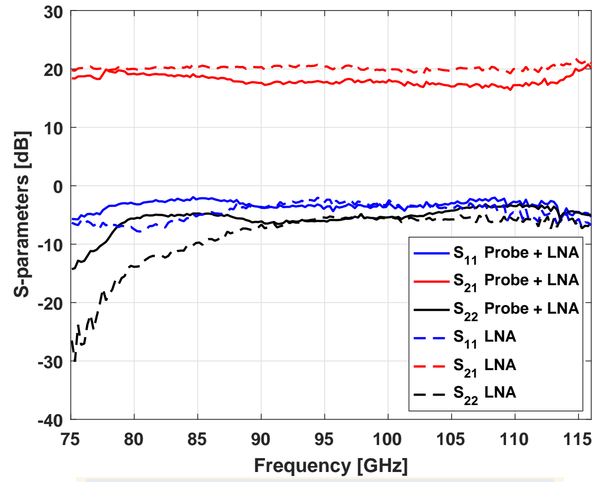


FIGURE 5.19: S-parameters of the full system simulation using alumina probe for flip-chip technique.

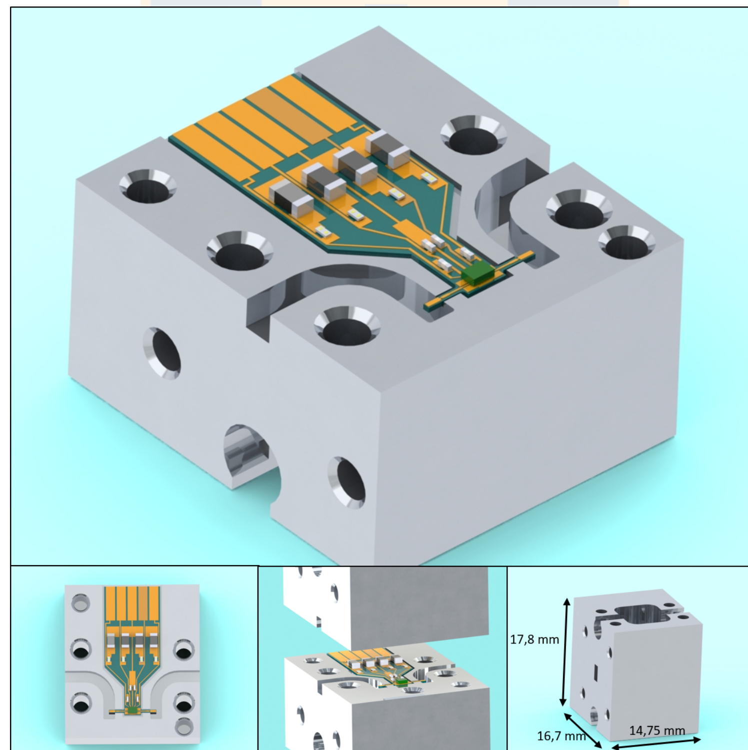


FIGURE 5.20: 3D solid model of the package along the PCB design from Fig. 5.18.

6

Design of 180-210 GHz InP/CMOS hybrid waveguide module interconnects

As mentioned in the motivation of this thesis, hybrid InP/CMOS solutions are attractive for low-volume, non-commercial applications. For water vapor radiometry or even planetary observations, for example. Hybrid InP/CMOS solutions allow taking advantage of the low noise of InP technology and the high integration that CMOS technology is presenting and also possibly with lower power consumption. These systems use CMOS System-on-Chip (SOC) with presiding low-noise amplifier InP [7]. This type of solution will make the miniaturization of technology possible by incorporating low-cost commercial technology. This technology has implementation challenges as seen in the previous chapter. Taking into account these challenges of CMOS technology, the aim of this chapter is to study techniques for waveguide packaging of InP/CMOS hybrid circuits operating at 200 GHz.

6.1 Indium phosphide and CMOS MMICs to package

The detailed design of the amplifiers were presented in [85] for the InP and in [5] for the CMOS. Fig. 6.1 shows a micrograph of both amplifiers, and their measured S-parameters are in Fig. 6.2. The InP MMIC LNA were designed in NGC's 35-nm InP MMIC technology and is a three-stage amplifier that uses a cascode stage at the output. The CMOS amplifier was manufactured with 32

nm Silicon-on-Insulator (SOI) CMOS technology and it has eight common source stages.

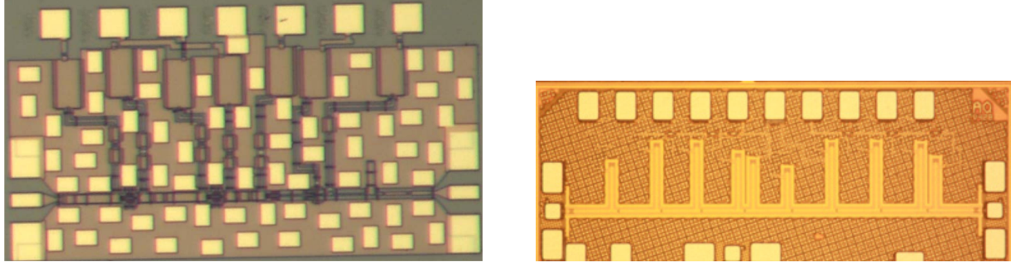


FIGURE 6.1: (left) Micrograph of the 160-270-GHz InP LNA [85]. (right) Micrograph of the 200-GHz CMOS amplifier [5].

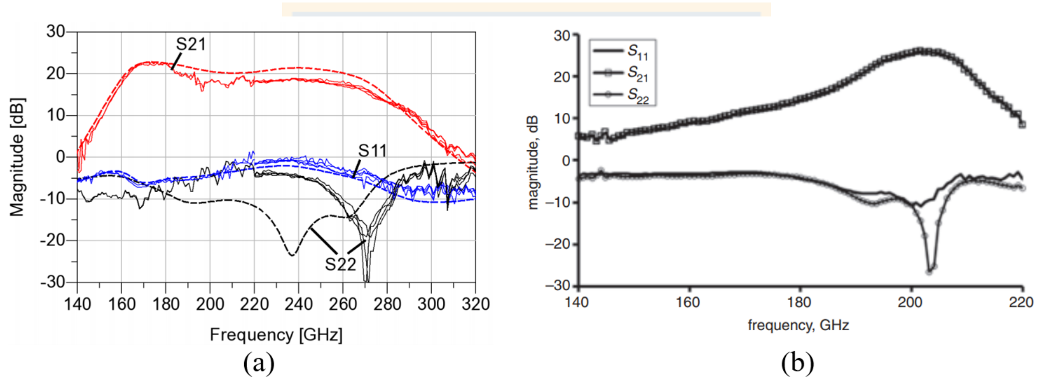


FIGURE 6.2: Measured S-parameters for the (a) 160-270-GHz InP LNA [85] and (b) 200-GHz CMOS amplifier [5].

6.2 Proposed interconnects for InP and CMOS technology connection

Three connection methods were studied: wire-bonds, flip-chip, membrane with quartz substrate, and membrane with silicon substrate. Fig. 6.3 presents a diagram of the setup for the simulations presented here. This setup begins with a WR-4 waveguide, followed by plane probe. It uses a high impedance inductive line in series with a low impedance capacitive line to tune the inductance of the wire-bond, see Fig. 6.4, [61]. This provides a 50-Ω match to the input of the InP amplifier. For the cases of wire-bond and flip-chip interconnections between InP and CMOS circuits, the output of the InP amplifier is connected by a wire-bond

to a microstrip transmission line that adapts it to 50 ohm, as the case of the input to the amplifier. Then, the connection between the output of the microstrip transmission line and the input of the CMOS amplifier is the one that will be used to carry out the study of interconnections. In the case of the membrane interconnection, the line that connects the output of the InP amplifier and the input of the CMOS amplifier is a CPW transmission line of the type used to perform this transition (see Section 2.3.3.3). In Fig.6.5, the four designs for the study of the InP/CMOS transition are shown. For each design, the pads model of the CMOS and InP amplifiers was used. Due to the high capacitive effect of the CMOS input pad, the effect of this PAD was de-embedded from the amplifier CMOS to perform the full simulation (Fig. 6.3).

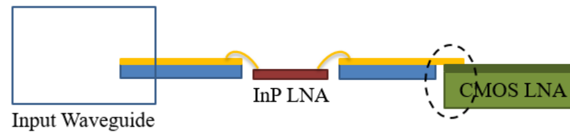


FIGURE 6.3: Set-up diagram for S-parameter simulations. In a circle, the connection that is under study using different types: wire-bonds, flip-chip and membrane.

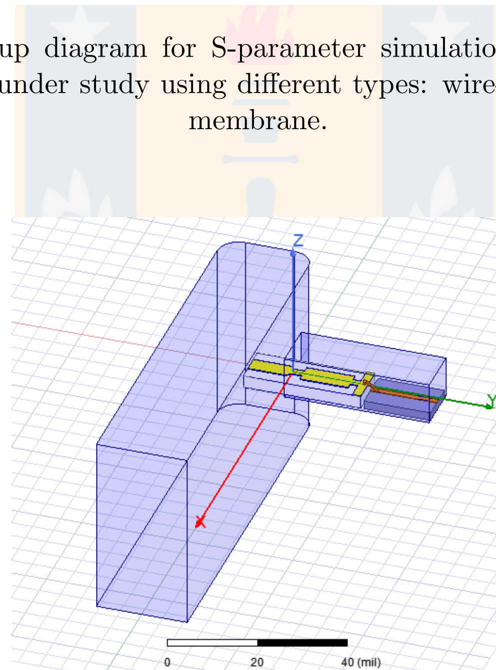


FIGURE 6.4: HFSS model of the E-plane transition, [61]. It is used for the input stage of the study model.

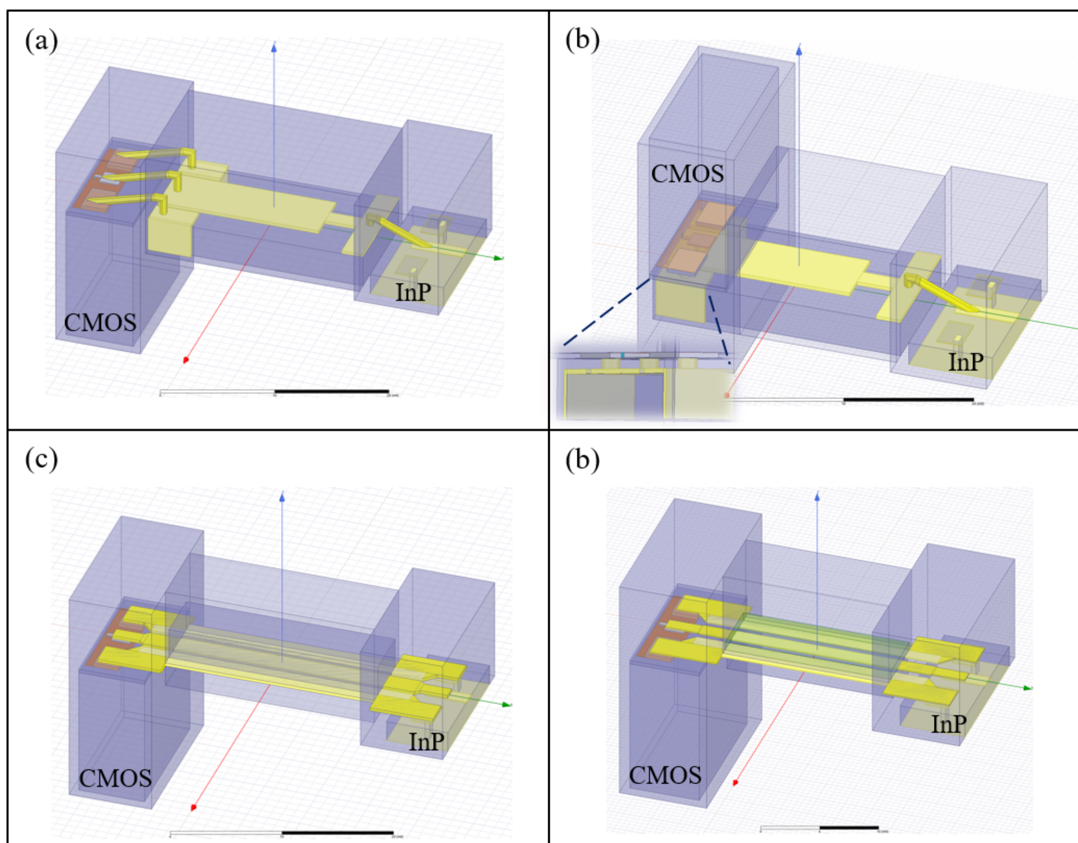


FIGURE 6.5: HFSS transitions models: (a) Wire-bonds, (b) flip-chip, (c) membrane using silicon substrate, (d) membrane using quartz substrate.

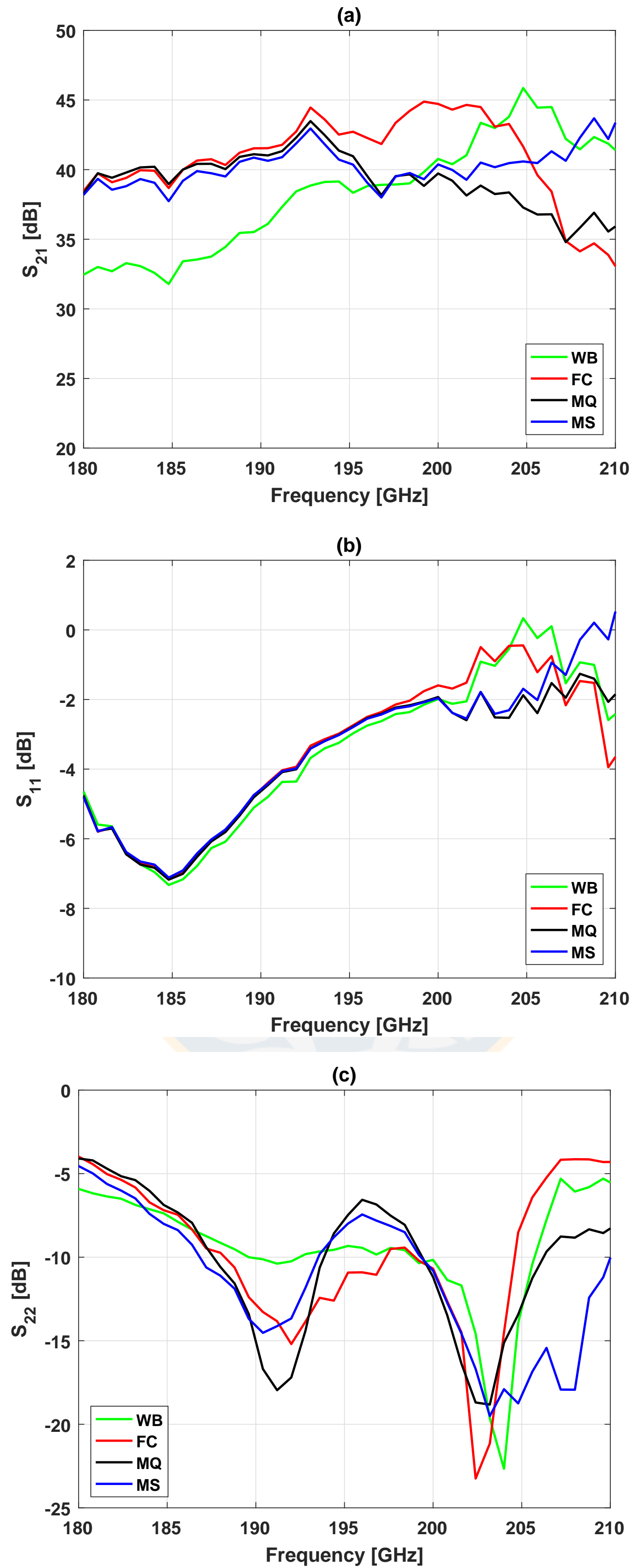


FIGURE 6.6: Simulated S-parameters for four types of interconnections between InP and CMOS amplifier: wire-bonds (WB), flip-chip (FC), membrane using quartz (MQ) and silicon (MS) substrate. (a) S_{21}, (b) S_{11} and (b) S_{22}

% referred to 180-210 GHz band	WB	FC	MQ	MS
% S_{21} over 40 dB	43	67	43	53
% S_{11} over -2 dB	27	17	13	20
% S_{22} below -10 dB	37	47	47	73

Table 6.1: Percentage of the frequencies band from 180 to 210 GHz in which an S-parameter is above or below a value. This table is based on the results shown in Fig. 6.6.

6.3 Results and conclusion

Interconnects for InP/CMOS hybrid solutions were presented for the 180-220 GHz frequency band. The interconnections studied were four: wire-bonds, flip-chip, membrane using silicon substrate and membrane using quarz substrate. Membrane using silicon substrate presented the relatively constant S_{21} values around 40 dB in the 190 to 210 GHz band. Flip-chip demonstrated the best S_{21} at 200 GHz with a value of 44.7 dB and it was a 67 % of the frequency band over 40 dB, see Table 6.1. This table presents a summary of the results. From the results obtained in this chapter, it is possible to establish that flip-chip and membrane are adequate techniques for the manufacture of packaging for the InP/silicon-based hybrid solutions at high frequencies.

7 Summary of the conclusions and future work

7.1 Summary of the conclusions

Silicon germanium technology demonstrated a steady operation under cryogenic room temperature in the 50 to 70 GHz band frequency. The noise performance improved in cryogenic conditions achieving a NF of 2.2 dB (191K) in the 52-65 GHz band frequency, which indicates an improvement factor of the noise temperature of 4.4 times less than at room temperature. The amplifier consumed 6.3 mW at its optimal cryogenic bias point. According to the authors' knowledge, this is the lowest value measured for a SiGe LNA in the 50-70 GHz band. This technology test sets a strong precedent for the future utilization of this technology as a second stage of amplification, or of an integrated receptor chip working under cryogenic temperature conditions. Packaging designs of a 75-116-GHz SiGe LNA were presented. These designs included the waveguide-to-microstrip probe transitions, the wire-bond and flip-chip interconnections, and the use of three materials as substrates: alumina ($\epsilon_r = 9.6$), AlN ($\epsilon_r = 8.8$) and megtron 7N prepreg ($\epsilon_r = 3.14$). Finally, an integrated design was presented, where the probes and a circuit of DC protections for the polarization bias of the circuit were integrated on the same PCB. A comparison was made between the wire-bond and the flip-chip using alumina as a substrate. The simulations for the interconnections by wire-bond presented a better performance at lower frequencies in the 75-110 GHz band as was expected, and they started to degrade their reflexion performance over 105 GHz and achieving 0 dB over 112 GHz. The flip-chip interconnection showed a better performance than the wire-bond in the same frequency band, maintaining the reflections nearly constant at around -5 dB up to the 105 GHz, where it starts

to improve achieving a level of -7 dB in the 115 GHz. The designs using AIN and megtron 7N, both with the flip-chip technique, obtained similar results to the ones obtained with alumina. This is due to the difficult matching of the highly capacitive impedance of the SiGe MMIC pads, and also due to the limitations imposed by the design rules of the manufacturers of the PCB. Preliminary simulations were carried out to verify the feasibility of making a hybrid silicon-based/InP solution in the band of 180 to 210 GHz. Four designs were presented, considering three types of interconnections between an amplifier of InP and one of CMOS. The interconnections used were wire-bond, flip-chip and membrane. For the latter, two types of substrate were used, quartz ($\epsilon_r = 3.8$) and silicon ($\epsilon_r = 11.6$), and quartz was used for the other two interconnections. The hybrid solution that presented the best gain was the one using flip-chip, with a 67 % of the frequency band over 40 dB. The input and output reflections were approximately similar, except for the membrane interconnections with silicon that was under -10 dB with a 73 % of the frequency band. The results presented in this thesis showed that:

- It is possible to use silicon-based microwave circuits in the millimeter waves at cryogenic temperature.
- The decrease in noise temperature of the silicon-base technology at cryogenic temperature is adequate to be incorporated in future cryogenic receivers of radio astronomy.
- The flip-chip technique is adequate to interconnect the silicon-based MMIC with the input and output probes. This is possible by obtaining a good performance for the W-band and providing the ground silicon-based MMIC, which has its pads on the surface of the chip.
- It is possible to integrate the InP technologies along with the silicon technology in a single packaging.

This last point will make the synthesis for the millimeter receivers possible for the implementation Earth remote sensing and radio astronomy. In this last implementation, the combination of the points before mentioned and added to the high integration functions that provide the silicon-based technologies, it will make it possible to synthesize the cryogenic millimeter receivers with hundreds of pixels.

7.2 Future work

Working on the implementation of the designs presented in Chapter 5 is necessary for their use at cryogenic temperature and have their noise performance verified. Additionally, the behaviour of the materials at these temperature levels should be verified. Possibly, studying also the effect of the repetitive thermal cycle of low temperature (cryogenic) of the flip-chip interconnectors. Thus, quantifying the reliability of the technology for its cryogenic use, which is possible to do for various types of substrate materials. This is aimed at finding the most adequate materials according to their thermal of coefficient expansion and that are of low cost. In addition, continue the progress of the InP/silicon-based hybrid technology. Managing to manufacture the packaging of two amplifiers in only one package could be a first step. Then, make progress towards the integration of chips with a high number of functions and a low noise. At this point, it is possible to continue on optimizing the development of the packaging and the transition circuits involved. An important aspect is to also move forward on the coordination of the MMIC designers and the packaging designers. This coordination is regarding the characteristic impedance of the circuits, and the physical and technological limitations that the packaging science is presenting at the frequency levels of millimeter waves. Lastly, continue on testing the technology based on silicon, at cryogenic temperatures, in order to analyze the behaviour of other types of circuits at these temperatures. As well as, continue on the optimization of the performance of silicon-based technologies using cryogenic transistor models.

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